PAYLOAD DESIGN REPORT

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<tr>
<th>Name &amp; Society</th>
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## CHANGE RECORD

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<th>Issue - rev</th>
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<tr>
<td>01 - 0</td>
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<td>• due to the high number of changes, they are not reported</td>
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LIST OF ACRONYMS

AEU      Ancillary Electronics Unit
AIT      Assembly Integration and Test
AIV      Assembly Integration and Verification
AOCS     Attitude and Orbit Control System
ASW      Application Software
BB       Bread Board
CAD      Computer aided Design
CCD      Charge Coupled Device
CNES     Centre National d’Etudes Spatiales
CTE      Coefficient of Thermal Expansion
DPS      Data Processing System
DPU      Data Processing Unit
DS       Detection System
EEPROM   Electrically Erasable Programmable Read-Only Memory
EGSE     Electrical Ground Support Equipment
EID-A    Experiment Interface Document (Part A)
EID-B    Experiment Interface Document (Part B)
ESA      European Space Agency
ESD      Electro Static Discharge
ESTEC    European Space Research and Technology Centre
FEE      Front End Electronics
FEM      Finite Element Model
FEU      Fast Electronics Unit
FM       Flight Model
FoV      Field of View
FPA      Focal Plane Assembly
GS       Ground Station
GSE      Ground Support Equipment
I/F      Interface
ICU      Instrument Control Unit
LEOP     Launch and Early Orbit Phase
LLI      Long Lead Item
LoS      Line of Sight
MEU      Main Electronics Unit
MGSE     Mechanical Ground Support Equipment
MLI      Multi Layer Insulation
MOC      Mission Operation Centre
OB       Optical Bench
OGSE     Optical Ground Support Equipment
PCL      PLATO Consortium Leader
P/L      Payload
PDAAS    PLATO Data Acquisition and Analysis System
PDC      PLATO Data Centre
PFM      Proto Flight Model
PI       Principal Investigator
PID  Proportional-Integral-Derivative (controller)
PIPD  PLATO Instruments Program Manager
PLATO  PLAnetary Transits and Oscillations
PLM  Payload Module
PMC  PLATO Mission Consortium
PPLC  PLATO Payload Consortium
ppm  part per million
PSF  Point Spread Function
QM  Qualification Model
ROM  Rough Order of Magnitude
SGSE  Software Ground Support Equipment
SRE-PA  Advanced Studies and Technology Preparation Division
SOC  Science Operating Centre
SM  Spare Model
SMM  Structural Mathematical Model
STM  Structural Thermal Model
SVM  Service Module
SWT  Science Working Team
TBC  To Be Confirmed
TBD  To Be Defined
TBV  To Be Verified
TC  Tele Command
TM  Telemetry
TMM  Thermal Mathematical Model
TOU  Telescope Optical Unit
TRP  Temperature Reference Point
UFOV  Unobstructed field of View
w/o  without
1. SCIENCE SUMMARY

1.1 MAIN GOALS OF PLATO

PLATO is the next generation planetary transit experiment; its objective is to characterize exoplanets and their host stars in the solar neighbourhood. While it builds on the heritage from CoRoT and Kepler, the major breakthrough to be achieved by PLATO will come from its strong focus on bright targets, typically with $m_V \leq 11$. The PLATO targets will also include a large number of very bright and nearby stars, with $m_V \leq 8$, as well as a large sample of cool M dwarfs down to $m_V = 15-16$.

The prime science goals of PLATO are:

1) Detection and characterization of Earth Analog systems.
2) Search for exoplanets around the brightest stars of solar type at all orbital periods and with all physical sizes.
3) Search for exoplanets around nearby M-type dwarfs with all physical sizes and at all orbital periods, including at orbital distances such that these planets fall within the habitable zones of these very cool stars.
4) Search for and characterization of exoplanets with a wide variety of sizes, masses and orbits around bright stars.
5) Full characterization of very bright stars, of all masses and ages, using seismic analysis.

The PLATO mission will detect and characterize exoplanets by means of their transit signature in front of a very large sample of bright stars, and measure the seismic oscillations of the parent stars orbited by these planets in order to fully characterize exoplanetary systems. These goals will be achieved by a long-term, ultra-high precision, high-time resolution, high-duty-cycle monitoring in visible photometry of bright dwarfs and subgiants, as well as of a large sample of M dwarfs. The PLATO observations will be complemented by ground-based follow-up observations, including radial velocity monitoring, which will be made easy and efficient thanks to the brightness of the PLATO targets.

1.2 SCIENTIFIC REQUIREMENTS

The science requirements of PLATO are detailed in the Scientific Requirement Document. They include the monitoring of five complementary star samples: the highest priority star sample includes more than 20,000 bright dwarfs and subgiants, typically up to $m_V = 11$, to be monitored for more than 2 (goal 3) years with a noise level better than 27 ppm in one hour. In addition to this main sample, the science goals of PLATO also require the monitoring of at least 1,000 very bright dwarfs/subgiants, with $m_V \leq 8$, of more than 3,000 dwarfs/subgiants with $m_V \leq 8$ for more than 5 months, more than 10,000 M dwarfs, and finally more than 245,000 cool dwarfs/subgiants for more than 2 (goal 3) years at a noise level better than 80 ppm/hr. Additional main requirements concern the duty cycle of the monitoring, which typically needs to remain above 95%, and a time sampling better than 50 sec for the highest priority bright star samples, and better than 600 sec for the fainter star samples.

The PLAnetary Transits and Oscillations of stars Mission (PLATO) will detect and characterize exoplanets by means of their transit signature in front of a very large sample of bright stars, and measure the seismic oscillations of the parent stars orbited by these planets in order to fully characterize exoplanetary systems. These goals will be achieved by a long-term, high-precision, high-time resolution,
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2. DOCUMENTATION

2.1 REFERENCE DOCUMENTS

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<td>RD1</td>
<td>PLATO Mission Requirements Document (MRD)</td>
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<td>RD2</td>
<td>PLATO – Assessment phase – PPLC design report PLATO.LAM.INS.REP.1044</td>
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<tr>
<td>RD3</td>
<td>PLATO Environmental Specification JS-23-09 (10 March 2010)</td>
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<td>RD4</td>
<td>Payload Requirement Specification PLATO.LAM.SYS.SPE.1064</td>
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2.2 APPLICABLE DOCUMENTS

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<td>AD1</td>
<td>Experiment Interface Document – A (EID-A)</td>
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<td>AD2</td>
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<td>AD5</td>
<td>PLATO Product Assurance Plan PLATO-MIAP-MP-14-CNES</td>
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3. MAIN CHARACTERISTICS OF THE INSTRUMENT

3.1 INSTRUMENT CONCEPT

The proposed instrument concept to meet all requirements of the mission is based on a multi-telescope approach, involving a set of 32 « normal » cameras working at a cadence of 25 sec and monitoring stars fainter than $m_V = 8$, plus 2 « fast » cameras working at a cadence of 2.5 sec, and observing stars in the magnitude range 4 to 8.

The cameras are based on a fully dioptic telescope including 6 lenses, protected against radiation effects by a front window; each camera has an 1100 deg$^2$ field, and a pupil diameter of 120 mm.
The 32 « normal » cameras are arranged in four groups of 8 cameras. All 8 cameras of each group have exactly the same field of view, and the lines of sight of the four groups are offset by a 9.2° angle from the +Z_{PLM} axis. This particular configuration allows surveying a total field of about 2250 square degrees per pointing, with various parts of the field monitored by 32, 24, 16 or 8 telescopes. This strategy optimizes both the number of targets observed at a given noise level and their brightness. It is assumed that the satellite will be rotated around the mean line of sight by 90° every 3 months, resulting in a continuous survey of exactly the same region of the sky.

Each camera is equipped with its own CCD focal plane array, comprised of 4 CCDs with 4510² pixels, working in full frame mode for the « normal » cameras, and in frame transfer mode for the « fast » cameras. The CCD working temperature is -65°C. The focal plane is cooled down through a thermal link with the telescope, the energy being radiated away by the baffle. The power dissipated by the front-end electronics linked to each focal plane is evacuated by the optical bench (PLM).

There is one DPU per 2 cameras performing the basic photometric tasks and delivering a set of light curves, centroid curves and imagettes to a central Instrument Control Unit, which stacks and compresses the data, then transmits them to the SVM for downlink. Data from all individual cameras are transmitted to the ground, where final instrumental corrections, such as jitter correction, are performed. The DPUs of the fast cameras will also deliver a pointing error signal to the AOCS, at a cadence of 2.5 sec. Several photometry algorithms (plain aperture photometry, weighted mask photometry, Line Spread Function fitting) are planned to run on board, each star being allocated one of them, depending on its brightness and level of confusion.

The selected concepts, and the dimensioning presented below, lead to an instrument with the following characteristics:

### 3.2 MAIN CHARACTERISTICS

<table>
<thead>
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<th>Characteristics</th>
<th>Value</th>
<th>Comments</th>
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<tbody>
<tr>
<td>Optics</td>
<td>Full refractive (6 lens + 1 window) design</td>
<td>Axi-symmetric design</td>
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<tr>
<td>Optics spectral range</td>
<td>500 – 1050 nm</td>
<td></td>
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<tr>
<td>Pupil diameter</td>
<td>120.0 mm</td>
<td>For one telescope</td>
</tr>
<tr>
<td>Normal telescope field of view</td>
<td>~ 1100 deg² / ~circular, dia 38.7 deg</td>
<td>For each telescope</td>
</tr>
<tr>
<td>Normal telescope detector</td>
<td>Full frame CCD 4510² x 18 µm square pixels</td>
<td></td>
</tr>
<tr>
<td>Fast telescope field of view</td>
<td>~ 550 deg²</td>
<td>For each telescope</td>
</tr>
<tr>
<td>Fast telescope detector</td>
<td>Frame transfer CCD 4510 x 2255 light sensitive 18 µm square pixels</td>
<td></td>
</tr>
<tr>
<td>Plate scale</td>
<td>15.0 arcsec / px</td>
<td>For both normal or fast telescope</td>
</tr>
<tr>
<td>PSF surface</td>
<td>Always included in 9 px</td>
<td></td>
</tr>
<tr>
<td>FPA equipment</td>
<td>4 CCDs in a square</td>
<td></td>
</tr>
<tr>
<td>CCD temperature</td>
<td>&lt; -65°C</td>
<td>By passive cooling</td>
</tr>
<tr>
<td>Parameter</td>
<td>Value</td>
<td>Notes</td>
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<tr>
<td>------------------------------------------</td>
<td>------------------------------</td>
<td>---------------------------------------------------------</td>
</tr>
<tr>
<td>Read-out frequency</td>
<td>4 Mpx / sec</td>
<td>For both normal or fast telescope</td>
</tr>
<tr>
<td>Read-out noise</td>
<td>55 e- rms / px</td>
<td>Global for detector and electronics, at nominal read-out frequency</td>
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<tr>
<td>Normal telescope CCD cycle period</td>
<td>25.0 sec fixed</td>
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<tr>
<td>Fast telescope CCD cycle period</td>
<td>2.5 sec fixed</td>
<td>To be confirmed with AOCS needs</td>
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<tr>
<td>Normal telescope exposure time</td>
<td>~ 22.0 sec fixed</td>
<td>+ a shorter exposure time for on-ground, at room temperature, tests</td>
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<td>Fast telescope exposure time</td>
<td>~ 2.3 sec fixed</td>
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<tr>
<td>Pointing error rate</td>
<td>2.5 sec fixed</td>
<td></td>
</tr>
<tr>
<td>Number of telescopes</td>
<td>32 Normal + 2 Fast</td>
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<tr>
<td>Power needed by payload</td>
<td>~ 820 W</td>
<td>Including 20% of uncertainties</td>
</tr>
<tr>
<td>Mass of the payload</td>
<td>~ 600 kg</td>
<td>Including 20% of uncertainties</td>
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### Characteristics | Value | Comments
--- | --- | ---
Payload field of view | Overlapping FoV of 2232 deg$^2$ | 32 cameras looking on 301 deg$^2$
 | 24 cameras looking on 247 deg$^2$ | 16 cameras looking on 735 deg$^2$
 | 8 cameras looking on 949 deg$^2$ | Equivalent pupil size | 678.8 mm for 32 cam | FEE and CCD activities are fully synchronised
 | 587.9 mm for 24 cam | 1 ICU with two processor/router and power supply in cold redundancy
 | 480.0 mm for 16 cam | 339.4 mm for 8 cam | Electronics | 1 FEE / camera
 | 1 DPU / 2 cameras | Science Operation Centre | ESA
 | 1 ICU with two processor/router and power supply in cold redundancy | Orbit type | Sun-Earth system L2 | Life time in orbit | > 8 years | Observation phases | 1$^{\text{st}}$ and 2$^{\text{nd}}$: 2 or 3 years | 1 pointing / phase
 | Eclipse | none | Step&stare phase | > 1 year | With several pointings
 | Attitude | 90° rotation around the LoS every 3 months | Lifetime in orbit | > 8 years

## 4. SYSTEM DESIGN

### 4.1 TOP LEVEL MISSION REQUIREMENTS

The main constraints are as follow:

| Maximal mass | General concept, number of cameras |
| Maximal power | General concept, number of cameras |
| Maximal TM volume | Type of data, number of stars to observe and then FoV size, number of cameras |
| Max. number of detectors | Max. number of cameras |
| Orbit around L2, attitude | Strategy of observation:
  - position of the Sun,
  - position of the planets,
  - rotation around the LoS every 3 months,
  - radiations type and dose |
Launch date: 2018 | General planning and critical components procurement. AIT of 34 cameras...
---|---
Life time in orbit of 6 years, with possibility to increase it to 8 years | • radiations integrated dose,  
• observing phases duration,  
• step&stare phase duration  
• optimisation of the FoV

4.2 DESIGN DRIVERS

The instrument is largely dimensioned by these three drivers:

− The instrument shall be limited by its photon noise, implying that each source of non-photonic noise shall remain below 1/3 of the photon noise, for stars fainter than $m_V=11$
− The periodic perturbations in the seismic observation range: [100 sec – 4 days] shall be reduced as much as possible,
− Observations shall be done as continuously as possible.

4.3 GENERAL

The PLATO payload is mainly based on the PPLC assessment phase study which we use as heritage for the technical concepts. Following the ESA recommendations at the end of the Assessment Phase, the total number of cameras has been reduced; payload has been revisited to reduce mass and the study limited to the payload.

The study during definition phase was consequently limited to the photometric chain which includes cameras and their digital electronics as defined in the next section. Optical bench, camera supports and sunshield are parts of the PLM and are completely excluded from the perimeter of our study.

The design of the cameras and the Data Processing System have been consolidated during this definition phase, to lead to the present design which is described in the following sections.

4.4 INSTRUMENT BREAKDOWN

The payload is composed by these following main sub-assemblies:

- 32 normal cameras, organized in four sub-groups. Each camera is composed by:
  - a Telescope Optical Unit (TOU): its mechanical structure supports the optical lenses and the baffle with various functionalities (thermal, straylight),
  - a Focal Plane Assembly (FPA), which supports the four detectors (CCDs in full frame mode), which also includes the 4 flexi-cables of the 4 detectors, to be connected on the FEE,
o the Focus Adjustment Shims (FAS) between TOU and FPA, used as the adjustment part to put the detectors at the best optical focus,

o the thermal equipment including: MLI at least around the FPA, and its I/F cables with FEE, the heaters and temperature sensors used for the camera temperature control and the temperature sensors used for monitoring the temperatures of various points on the camera,

o the Front End Electronics (FEE) box, located close to the FPA, including mainly the 4 video chains, the CCDs phase drivers and the temperature sensor acquisition and conditioning.

- 2 fast cameras, with similar sub-systems called fast TOU, fast FPA, fast FEE..., differing from normal cameras by a reduced bandwidth of the normal camera optics (to provide a chromatic photometry), and use of the same detector but in frame transfer mode (to provide the position error information to the SCAO).

- electronics, composed by:

  o Ancillary Electronics Units (AEUs), mainly composed by the DC-DC converters used to power the associated FEE, and the synchronisation board used to have a fully synchronise acquisition by all the cameras. Physically, they are grouped together in 5 boxes, 4 for normal cameras, and 1 for fast cameras,

  o Data Processing Unit (DPU). Functionally, each is associated to 2 FEEs. Physically, they are grouped together by 4 in the same box called MEU. We will have then 4 MEUs (16 DPUs) for the 32 cameras. Each of these boxes includes its power supply.

  o Fast DPU, functionally associated to the fast FEE, one for each. We have then 2 Fast DPUs, each associated to its fast camera. The 2 Fast DPUs are grouped in one box called FEU, also including its power supply.

  o 1 Instrument Control Unit (ICU), with 2 complete processor/router chains used in cold redundancy, and then functionally completely independent, with their power supply.. Each, if active, can exchange data with all DPUs, all Fast DPUs, and with the SVM. The 2 ICU are grouped in a single box with their power supply.

- on-board software, located into DPUs and ICUs, which can be modified during the flight.

- harnesses which will be provided by the consortium correspond to:

  o the flexi-cables for the detectors between FPA and FEE,

  o the harness dedicated to temperature monitoring going from temperature sensors in various locations on each camera structure to its FEE.

  o the harness between the heaters, temperature sensors used for camera thermal control, and a connector located close to the camera.
• other harnesses which will be electrically defined by the consortium but provided by the contractor correspond to:
  
  o all (except those listed above) instrument-relevant interconnecting harnesses,
  
  o all instrument to SVM connecting harnesses.

The cameras are located inside the PLM, protected from the Sun by the sunshield (satellite part). The electronics can be located either in the PLM or in the SVM.

Then, by definition:

• a telescope is the unit including the optics, the barrels, the support structure, the dedicated baffle and the dedicated thermal hardware

• a detection subsystem is a FPA + FEE + related harness

• a camera is a subassembly which includes a telescope and a detection subsystem. It is powered by an AEU, which is strictly not part of the camera

• the DPS includes: MEUs, FEUs, ICUs, and related software

• an instrument is the full functional chain including a camera, and all the electronics and software associated to the camera and internal harness up to the interface with the SVM.

• the payload is the full set of instruments.

4.5 MAIN CHANGES SINCE THE ASSESSMENT PHASE

We have conserve the concept resulting on trade-offs made during the assessment phase. The instrument is then based on the multi-telescope concept and a dioptic design.

To maintain the performances of the payload with a lower number of cameras, we have enlarge the FoV of the camera, and for that, we have optimize the optics and increase the size of the detectors. This optimisation has led to a new design which has, with 32 normal cameras, performances similar to the assessment design with 40 normal cameras.

In parallel, the optical design has taken into account the radiations effects and a preliminary thermal analysis has led to introduce a window in front of the objective, for:

• limiting the darkness of the optics with the radiation cumulated dose,

• decreasing the temperature axial gradient inside the telescope.

The increase of the FoV has led to re-visit the overlapping factor used during the assessment phase to take into account the new size and shape of the camera FoV.

DPU’s activity was consolidated since the assessment phase authorising presently the use of only one DPU per two cameras (instead of one DPU per camera previously).

All these new updates are compatible with the mass and power constraints imposed to the payload by the satellite.
4.6 OPTIMISATION OF THE PHOTOMETRIC CHAIN

4.6.1 SIGNAL BUDGET

The signal budget is unchanged since the answer of the AO, except a small change in the CCD coating reference. It was re-visited for the AO answer, to take into account:

- the presence of a window, in front of the 6 lens objective,
- the decrease of the wavelength bandwidth, resulting from the need of preserving the global performances with a lower number of cameras: larger FoV with the same PSF characteristics,
- the use of the “Gaia like” coating on the CCD, which is slightly better than the red enhanced coating previously used,
- and the decrease of the exposure time resulting from the selection of new enlarged detectors, and CCD line transfer time higher than required.

Details of this budget are given in the Payload Performance Report [AD4].

4.6.2 FIELD OF VIEW

Once the pupil size is selected, the focal length is limited by the speed of the optics. An f ratio of f/2.0 is considered as an absolute limit before a large increase in the optical design complexity.

The new optical design can supply “good” PSF (compliant with the requirements) up to 19.3° (TOU requirement) from the camera axis.

Then, the field of view is mainly limited by the geometry of the detector. The FPA is considered as a square fit out with 4 square CCDs, each with 4510² square pixels of 18 µm side.

This yields a circular field of view with a diameter of 38.7°, slightly limited by the 4 edges of the FPA to 36.6 x 36.6° totalising a theoretical value of ~115 0 deg² for the field of view. By removing the loss due to the gap between the sensitive areas of the different CCDs, the useful size of the field of view becomes 1108 deg². Corners of the FPA are then in fact vignetteed by several parts and are then considered as giving bonus observation FoV. The value taken for star count performance is then this last value of 1108 deg².
4.6.3 OVERLAPPING FIELD OF VIEW

4.6.3.1 DRIVERS

The main driver for choosing the instrument basic configuration is related to the need to optimize simultaneously the number and the brightness of observed cool dwarfs and subgiants. The concept of overlapping field-of-view, offering a very wide field of view covered by a variable number of cameras, was a natural consequence of this main idea.

In addition to this basic motivation, the overlapping field-of-view allows us to re-observe, during the step&stare phase, some stars for which particularly interesting planets were detected in the long monitoring phases of the mission (in particular for instance telluric planets in the habitable zone), but only with a sub-set of telescopes, therefore without reaching the required photometric precision for seismic analysis during these phases. During the step&stare phase, these targets can be put in the part of the field observed with all the 32 telescopes, thus reaching the best photometric precision, giving us the potential to fulfill photometric requirements.

4.6.3.2 DESIGN

The overlapping field of view is obtained by use of 4 sub-groups of cameras, each with 8 cameras, all the cameras of one sub-group have the same LoS, and the 4 sub-group LoS are tilted by a value of 9.2° from the Z axis of the PLM.
Tilts of the LoS of the different sub-groups

On the following sketch, each disk represents the FoV of a sub-group, each offset by 9.2° from the Z_{PLM} axis (centre of the figure), and the resulting FoV of the payload is then composed of 4 zones, seen by various numbers of cameras: from the pale at the centre (32 cameras) to the dark in the 4 angles (8 cameras):

Payload overlapping FoV

The result is an instrument with a larger field of view than a single camera, with various pupil sizes:

- The centre, seen by the 32 cameras, offers the largest pupil size, but is limited in size to 308 deg²,
• A second zone, seen by only 24 cameras, offers an intermediate pupil size on a FoV of 252 deg².
• A third zone, seen by only 16 cameras, offers therefore an intermediate pupil size on a FoV of 750 deg².
• And a fourth zone in the corners of the FoV, seen by only 8 cameras, with the smallest pupil size, and also on a FoV of 969 deg².

4.7 SIGNAL CHAIN DIMENSIONING

4.7.1 NORMAL CAMERA

The detector saturation level is linked to the pupil size, optical transmission, exposure time, full well capacity (FWC), PSF size and shape, Q.E of the CCD, and star brightness.

With the pupil size selected and the PSF size largely constrained by confusion issues, a special effort was made on the CCD for a large increase of the FWC, in order to improve the access to low magnitude stars, which are of major interest for science.

Moreover, the preparation of Corot has shown the possibility to exploit photometrically slightly saturated spots, an option which Kepler is using extensively as well. For PLATO, this possibility will also be used to increase the useful magnitude range.

The dimensioning of the signal chain is such that saturation occurs near magnitude 8.0 for normal cameras, further assuming that one magnitude brighter targets can be observed by working on saturated images.

4.7.1.1 CCD FWC

After consultation of the e2v engineers, the FWC can be increased to 900 or 1000 ke-/px by a modification of the oxide layer thickness. This modification seems possible for a new component, with a good control of difficulties, risks and delivery impacts.

Our work base for the FWC is then this value of 900 ke-/px.

4.7.1.2 CCD READOUT TIMING

The CCD cycle period (exposure and frame reading time) shall be:

- shorter than the 50 s sampling time required by the science,
- and longer than 20 s, which is the acceptable limit for the additional photon noise introduced by smearing (which must remain below 1/3 of the target photon noise),
- detector saturation shall be under control to avoid loss of bright stars data.
Adopting an integer fraction of the sampling time for the cycle period, which is an optimum for data volume and handling, we can select 25 or 50 s for the cycle time:

- 25 s gives a saturation magnitude close to 8.2 with the nominal pupil diameter of 120.0 mm, depending on the position in the field. The requested magnitude of 8.0 gives spots slightly saturated in some positions but still acceptable for the photometry calculations by use of special binary masks. To reduce the data volume, two successive images can be added in the DPU to give data with a sampling time of 50 s.

- 50 s corresponds exactly to the required sampling time, cancels the need of data addition in the DPU, reduces the smearing rate, but gives a saturation magnitude close to 9.2 with the same assumptions as before on the PSF size and shape. Such a saturation magnitude is unacceptable compared to the science needs.

The cycle period of 25.0 s is taken as our baseline.

4.7.2 FAST CAMERA

The fast cameras have three main purposes:

- provide photometry of extremely bright stars (mV< 8.0). To this end, the exposure time shall be sufficiently low to avoid a saturation of the detector for these bright targets,

- provide the capacity to observe in two colours, with two broadband filters,

- provide the data needed to compute pointing angle error for the AOCS. These data shall be supplied to the AOCS at a high frequency rate to reach the pointing performances. A CCD cycle period (exposure time + frame transfer time) of 2.5 seconds seems, from our point of view, a maximum acceptable for the AOCS needs, and is compatible with the image reading rate.

This timing, coupled to a frame transfer time shorter than 0.3 s, gives a saturation magnitude of about 4.8.

The baseline is a CCD cycle period of 2.5 seconds for the fast cameras, but can be re-considered up to a confirmation by the AOCS specialists.

4.8 MECHANICAL ARCHITECTURE

4.8.1 GENERAL NEEDS

The mechanical architecture of the payload is driven by the following considerations, resulting from optical, thermal and mechanical constraints. Mechanically, the considerations are the following:

- all 34 cameras must be as far as possible identical
- they must be independent (only linked by the PLM optical bench)
- the link of the telescope to the optical bench (or a camera support) must be isostatic, and shall ensure an orientation of the camera around its optical axis
any camera must not obstruct the FoV of any other camera  
the 32 normal cameras are grouped in 4 sub-groups of 8 cameras with a common LoS  
the 2 fast cameras are co-aligned with the $Z_{PLM}$ axis  
the inner surface of each individual baffle shall not see the sunshield for both thermal and stray-light aspects  
each camera (excluding its FEE) should be as far as possible thermally uncoupled from other cameras and from all satellite structures  
the FEE shall be close to its associated FPA, and then, located “under” the FPA for the need of 34 cameras accommodation.

The global architecture is imaged in the following sketch:
4.8.2 SKEW SPACER (OR CAMERA SUPPORT)

The tilt of the normal cameras with reference to the PLM reference (9.2°) is given by a specific part: the skew spacer, supplied by the satellite contractor. This part interfaces the cameras and the optical bench. The orientation of the camera I/F plane can be obtained directly by manufacturing or by addition of shims which could be used for adjustments of the camera axis with reference to $Z_{PLM}$ axis. One can also note that the skew spacers are all identical: only their orientation around $Z_{PLM}$ axis changes as a function of the direction of the tilt. We have four angular positions of these spacers $0$, $\pi/2$, $\pi$ and $3\pi/2$ rad.

4.8.3 CAMERA INTERFACES

All the cameras are externally identical and their interfaces are all the same. They are fixed on the previous skew spacer via 3 bipods positioned at 120° around $Z_{CAM}$ axis (see the TOU mechanical design in the next section). These three bipods are strictly identical for avoiding the tilt of the cameras during temperature decrease.

4.8.4 THE BAFFLES

The baffles are mainly needed for the thermal control of the camera. Their external surface is insulated (MLI) from the radiations of other cameras and from all other surfaces of the payload. Their internal conical surface is used as a radiator toward space. This is the reason why their higher end "is cut by the plane of the sunshield" that makes an angle of 30° wrt the XY$_{PLM}$ plane. As a direct consequence, the position along $Z_{PLM}$ of a camera depends on its position along $X_{PLM}$ axis (see $H_1$ and $H_2$ on previous figure). Since these heights also depend on the height of the baffle, we see that the location of the camera is over-constrained: it is fixed on the skew spacer at its base and is in a fictive contact with the sunshield plane at its top. This confirms two things: 1° this interface must be managed with precaution 2° the capability of an adjustment of the height must be kept (a priori as we said before, with shims at the surface of the skew spacers). Finally, one can add that there are three different shapes for the baffles: one for fast cameras and only two for covering the four different tilts of normal cameras. Indeed, the cameras that are tilted symmetrically wrt the $XZ_{PLM}$ plane have identical baffles.
We give in the table here after the values of two angular characteristics of the three baffles: the first angle is the cutting angle of the baffle measured in its symmetry plane (noted $\chi$ on figure below). The second angle is the orientation of the baffle around the optical axis (it is noted $\xi$ on previous figure). It is measured as the angle between the symmetry plane of the baffle and the plane $XZ_{\text{CAM}}$.

<table>
<thead>
<tr>
<th></th>
<th>Cutting angle</th>
<th>Orientation around $Z_{\text{CAM}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fast Camera</td>
<td>30.00°</td>
<td>0</td>
</tr>
<tr>
<td>Normal Type 1 &amp; 4</td>
<td>37.03°</td>
<td>$\pm 9.05^\circ$</td>
</tr>
<tr>
<td>Normal Type 2 &amp; 3</td>
<td>24.30°</td>
<td>$\pm 14.23^\circ$</td>
</tr>
</tbody>
</table>

These angles are only dependent on three parameters: the angle of the sunshield ($30^\circ$), the tilt of the cameras ($\pm 9.2^\circ$) and the angle that makes the tilt axis with the $X_{\text{PLM}}$ axis ($\pm 45^\circ$). These three angles are imaged on following sketch.
4.8.5 THE FEE BOX

This electronic box is located approximately at 65 mm below the bottom of the focal plane assembly, length which is compliant with the required free length of CCD flex-cables. It is mechanically linked to the PLM, not to the camera. Then, there are 2 possibilities for its fixation: the box is fixed on the OB or it is fixed on the skew spacer. In both cases, it shall have the same orientation as the camera, since the flex-cables of the 4 detectors have the same length. Then, a large misalignment of the FEE box or a different orientation with reference to the camera is to be carefully checked with the flexibility of these flex-cables.

4.9 THERMAL ARCHITECTURE

4.9.1 THERMAL NEEDS DURING OBSERVATION PHASES

4.9.1.1 THERMAL NEEDS FOR THE CAMERA DURING OBSERVATION PHASES

The main issue is to cool down the FPA, and evacuate its power. Since it is impossible to evacuate the power along the transverse axes of the camera, due to the presence of neighbouring cameras, and also impossible on the backside (-Z\text{CAM} axis) due to the presence of the video electronics and the optical bench, then the only remaining axis for power evacuation is the +Z\text{CAM} axis, by the way of the baffle seeing the sky. The structure of the telescope shall then be highly conductive for temperature gradient limitations, and the baffle dimensioned for the evacuation of the FPA and leaks by radiation.

The temperature of detectors is selected as lower than -65°C, for dark current and radiation effects limitations.

In other respects, the optics is necessary cold, because:

- The front window sees the sky under a large solid angle and is cold,
- The last lens which is close to the cold detector and is also cold,
• A thermal gradient inside the optics is not welcome for performance aspects.

Then, the optics is necessary cold, and its temperature is fixed to -80°C, measured at its TRP, compatible with the selected temperature of the detectors.

The main functions of the camera (w/o FEE) thermal system are then:

• to maintain the optics at the selected temperature measured at the camera TRP,
• to maintain the FPA under its maximal authorised temperature.

Moreover, the performances of the camera are strongly linked to its temperature stability. To facilitate the thermal stability, the following concept is adopted:

• the camera (w/o FEE) shall be strongly isolated from temperature variable (or not controlled) sources (sunshield inner surfaces, optical bench...). The fixation bipods of the camera and the flex-cables between FPA and FEE have then a low thermal conductance, and MLI is installed on critical surfaces for radiative coupling limitation. The FEE is cooled by another way which could be the optical bench, managed by the satellite contractor.

• the power dissipated inside the FPA is fixed on timescales higher than 25.0 sec. The cycle time and exposure time of the CCD are then fixed.

Moreover, it is request to have the possibility to slightly change the camera temperature to optimise its working point on criteria of the best PSF size and shape. This can be realised by controlling its temperature in a small range around its nominal working temperature: presently [-75°C, -85°C] is required, but this range could be extended: effectively, recent optical studies on performance variations with temperature have shown that optical design can deliver good PSF (in the requirements) in a range of +/-10°C around -80°C. This new information is not taken into account for now, but it could be, as it has low impact on requirements and studies, and would lead to a more robust and safer instrument.

4.9.1.2 THERMAL NEEDS FOR THE OTHERS EQUIPMENTS DURING OBSERVATION PHASES

What is required to temperature control (ensured by SVM) during observation phases is to maintain the electronics boxes in their operating temperature ranges, within a given temperature stability.

These ranges and stabilities are given in the EID-B.

4.9.2 THERMAL NEEDS DURING OTHERS PHASES

What is required to temperature control (ensured by SVM) during all the phases except the observation phase is to maintain the equipments inside their operating temperature ranges. During these phases, the temperature stability can be largely relaxed.

These ranges and stabilities are given in the EID-B.
4.9.3 THERMAL CONTROL

The temperature control is entrusted to the SVM, mainly by the fact that the temperature of the equipments shall be controlled during all the phases of the mission, even when they are not powered.

For the camera (without FEE), it is required to SVM a temperature control by PID controller at the camera TRP. On the instrument side, heaters and temperature sensors will be installed. The control loop stability will be checked by use of an equivalent PID controller during thermal test of the camera, and its characteristics given to the satellite contractor. The contractor is in charge to supply the flight controllers, one per camera, and the verification of the entire temperature control.

Performances required to temperature control are written in the EID-B

4.9.4 TEMPERATURE MONITORING

Fully independent of the temperature control, the temperature monitoring consists in the measure of the temperature in several points on the camera, by the use of high resolution sensors, in limited temperature ranges. By this way, we can monitor the temperature variations with a very high sensitivity, due to this high resolution, and the time oversampling.

The typical resolution which is required for these sensors and their acquisition-conditioning system is 2-5mK / LSB or better (TBC), with a sampling rate of 1 sample/6.25 sec for normal cameras and 1 sample / 2.5 sec for fast cameras. These sensors located on the camera structure are acquired and conditioned by their associated FEE, before their addition in the header of image data and a sending to ground by the same way as the image data. This allows the possibility to reach temperature variations as low as 0.1 mK by use of filtering or averaging on timescales in the order of minutes.

4.9.5 CAMERA THERMAL CONFIGURATION

4.9.5.1 CONFIGURATION

With these above needs and requirements, we arrive on a thermal architecture with:

- a FPA and a telescope structure strongly connected (on thermal aspects).
- the inner surface of the baffle has a good emissivity (black anodise).
- the coupling between baffle and structure can be used as a parameter for temperature range trimming.
- this unit (FPA + telescope structure + baffle) is isolated as highly as possible from the rest of the satellite and the sky.
- the fixation bipods and the flex-cables between FPA and FEE have thermal conductivities as low as possible.
- baffle outer surface, telescope structure, FPA, bipods and FEE top surface are covered by MLI, for radiative flux limitation.
- heaters and sensors for temperature control are wired in a bundle ending on a connector (which could be mechanically supported by the OB) used as I/F with the SVM cable.
- temperature sensors used for monitoring are wired in a bundle ending on a connector to plug on the FEE.

### 4.10 ELECTRICAL ARCHITECTURE

#### 4.10.1 DIGITAL ELECTRONICS

Digital functions are implemented into several units: the CCD image processing is performed by either the normal DPUs (located in the MEUs) or by the fast DPUs depending on the cameras (either normal or fast). Then all the data processed by the DPUs are transmitted to the ICU for additional treatments. Each MEU hosts also two SpaceWire routers to merge the data from the 4 N-DPUs. A SpaceWire router unit is also implemented in each ICU to merge data from the 4 MEUs and the 2 Fast DPUs (following figure). In order to improve the SpaceWire network redundancy scheme, the SpaceWire router unit of the ICU-A and the SpaceWire router of the ICU-B can be switched on simultaneously by the active ICU Processor Unit, and then work in hot redundancy.

For commandability and monitoring purposes, the 4 normal AEUs and the F-AEU, are also connected to the SpaceWire network.

The diagram below shows the nominal and redundant SpaceWire network.
SpaceWire network architecture
4.10.2 DATA FLOWS

As shown in the figure above, due to the large number of cameras the data flow architecture is hierarchical: each camera owns its front end electronics (FEE) in charge of the readout of the four CCDs of a FPA. Therefore each FEE includes a phase sequencer, 8 analog processing and 14-bit digitization electronics as well as adjustable biases.

In addition each N-FEE includes two high performance SpaceWire bidirectional serial interface 1- to transfer to the digital electronics the digitized CCD raw data 2- to receive from the digital electronics low level commands (mainly to configure the analog electronics) and 3- to transfer digital housekeeping to the ICU via the MEU. Digital data are then processed in the N-DPU sub-systems of the MEU.

In addition each F-FEE includes 8 SpaceWire bidirectional serial interfaces 1- to transfer to the digital electronics the digitized CCD raw data 2- to receive from the digital electronics low level commands (mainly to configure the analog electronics) and 3- to transfer digital housekeeping to the ICU via the F-DPU Digital data are then processed in the F-DPU.

Refer to section 5.11 for a full description of the data processing. When processed the digital data are gathered by the ICU which in charge of the generation of telemetry packets towards the SVM mass memory.

Similarly, all sub-system housekeeping parameters are gathered by the ICU which is in charge of generating corresponding telemetry packets and eventually performing actions related to instrument FDIR.

Bidirectional data transfer between DPU and ICU is achieved by mean of 4 (MEU) + 2 (fast DPU) SpaceWire links.

4.10.3 COMMAND DISTRIBUTION

Configuration commands are received by the ICU from the SVM. Then according to the destination, the command is processed and routed either to MEU, F-DPU, N-AEU, or F-AEU (see figure above). Finally the command is routed to FEE (through DPU) when applicable.

4.10.4 CLOCK AND SYNCHRO DISTRIBUTION

4.10.4.1 GENERAL SYNCHRONISATION CONCEPT PHILOSOPHY

PLATO has the double particularity to be a very high accurate relative photometer and to have a science bandwidth at very low frequencies. The resulting need is here to a very low instrumental noise in the science frequency bandwidth, in terms of random noise or parasitic lines, fixed or slightly moving in the Fourier spectrum. For this last need in particular, the resulting constraint is to limit the number of various oscillators, each with its own frequency to avoid or limit the risk of beating between these oscillators.

We cannot take the risk to use several oscillators located in the FEEs of all cameras. Effectively, the level of noise required at instrument level is very low, an EMC coupling between two electronics boxes or between cables at such low levels is inevitable and could be not seen during EMC tests at ambient
temperature and consequently with a poor sensitivity on the detector. This could be a high risk of damage in the performances for the two scientific programs.

Then, the general philosophy for the instrument is to synchronise all the activities especially on low level analog electronics: detectors, attached video electronics and their power supplies, and in their close environment (camera active thermal control). With this precaution, an eventual EMC coupling between two or several subsystems, will only results on a fixed pattern in the data, which can be managed like others stable perturbations.

4.10.4.2 SYNCHRONISATION SIGNALS

All the activities of the cameras are synchronised by a unique reference clock distributed to all sensitive boxes: FEEs (normal and fast), AEU (normal and fast), detectors (by the way of FEEs) and active thermal control.

Two synchronisation signals are needed:

- a reference clock signal at a high frequency, which is used by the master FPGA located inside the FEE as its frequency reference. This FPGA manages the activity of the CCD (frame transfer, line transfer, pixel readout, reset, DC-restore signal…) and of the video electronics (clamp, start conversion…).

- a "PPS" signal at a lower frequency, which gives the start signal to all cameras, and marks out the first detector readout start.

4.10.4.3 SYNCHRONISATION REALISATION

For now, these two signals are delivered by the SVM to the N-AEU and F-AEU boxes (one main and one redundant). The SVM on its side, in case of use of PWM amplifiers for heating the cameras (temperature control), can synchronise this activity, on the same signals. On PLM side, AEU receive the signals, and transmit them to FEEs, which are using them for synchronising all the CCDs. The camera activities are by this way fully synchronised.

As an alternative solution we are now proposing to have a low power, low mass and then "small" box located close to the centre of the optical bench (as proposed during the assessment phase), only including reference oscillators (M and R), frequency dividers, commutation logic for switching on main or redundant chain, and lines drivers for sending the needed synchronisation signals intended for N-AEU and F-AEU, N-FEEs and F-FEEs. This box could be commanded and controlled by the ICUs, and powered by the F-AEU (main and redundant power supplies). If needed, a double line (M and R) will send the synchronisation reference signals to the SVM for heating system synchronisation. The N-AEU and F-AEU are then using these signals to synchronise them-selves at a frequency close to 125 kHz. (See following figure)
Third solution: to avoid having a box which needs to be cooled close to the optical bench, it could be installed inside the SVM, close to the other electronics boxes, with a similar cabling as presented on the previous figure, but with different cable lengths. This box could stay a independent box, or could become a function included in the F-AEU. For both cases, the main advantage is a cleaner optical bench without need of additional cooling, and the penalty is longer cables carrying high frequency signals to the cameras.

In all the cases, the boxes will use LVDS line drivers or receivers, to transmit or receive the high frequency signals which will be carried on twisted shielded pairs as SpaceWire signals.
4.10.5 POWER DISTRIBUTION

Secondary power generation for the analog electronics is concentrated in the AEU units. Each unit hosts a bench of 5 independent DC/DC converters (one converter per telescope). Each AEU has a redundant interface with a platform regulated power line (see figure below). Secondary power generation for ICU and F-DPU is performed locally in each unit.

4.10.6 REDUNDANCY CONCEPT

In order to mitigate the impact of electronic unit or function failure, we need to optimize the reliability figure of the instrument.

The first principle is to suppress whenever possible the identified single point failure: in other words the aim is to avoid the loss of the complete instrument due to a failed function.

The ICU function is at the heart of the payload, and loosing this function would imply loosing the whole payload. So the ICU function is redunded. Therefore, the ICU function is divided in three sub-functions: Power Supply of the ICU function, Processing function and Router function. These 3 sub-functions are redunded and cross-strapped.

Second, when redundancy is not applicable the principle is to split the functions into sub-sets in order to limit the effect of a failure by limiting its propagate on. Analog electronics and associated power converters rely on this type of architecture: rather than having a single large DC/DC converter to feed all
the FEEs, a bench of DC/DC is foreseen. In case of a failure of one of the FEE (e.g. over-current) only the corresponding DC/DC converter is affected. This can be easily managed by current limiter in the converter.

Thermal control lines, comprising 3 temperature sensors, use the median value for feedback power to two redundant heaters.

The general philosophy we have adopted is:

One failure in a normal equipment (as example an AEU) can affect only one normal camera with the risk of loss of this camera.

Two failures in the same normal equipment can affect more than 1 normal camera.

The two fast chains are fully independent, and one failure in a fast equipment can affect only one chain with the risk of loss of this fast camera.

4.10.7 INTERNAL INTERFACES

See EID-B

4.10.8 EXTERNAL INTERFACES

See EID-B

4.11 DATA TREATMENT ARCHITECTURE

4.11.1 DATA PROCESSING ALGORITHMS

The final goal of the data processing is to provide light-curves that fulfil the requirements in terms of white noise and coloured noise. Due to the limited bandwidth of the telemetry, the photometry of the targets (i.e. the light-curves) must be performed on-board. Because the performances of the DPUs are too limited to perform a 2D PSF fitting, simpler algorithms such as mask photometry are base-lined.

4.11.1.1 PERTURBATIONS AND SOURCES OF NOISE

We list here the perturbations and sources of noise that have been identified so far as having an important impact on the quality of the data.

Confusion: Stars fainter than around magnitude 11 are expected to be perturbed by fainter stars (contaminants). Three different types of perturbations are identified: photon noise from the contaminants, combined effect of confusion and satellite jitter (see below), and the flux of the contaminant introducing a bias on the measurement of the depth of transit and for seismic analysis.

Kinematic differential aberration: Due to the relativistic effect related to the satellite motion with respect to the stars, the angle between two stars varies with time. Since the total FOV is as large as 50°, the variation of the angle between two stars located in two extreme positions of the FoV is expected to be
up to around 35 arcsec in three months (worst case). If we consider a pixel size of 15 arcsec, this motion corresponds to a displacement of up to around 2.3 pixels per three month (worst case). These displacements will obviously induce a decrease of the star flux. Furthermore, after three months (worst case), the stars located far from the direction of the LoS of the satellite will go out of their mask.

**Thermo-elastic differential aberration:** thermo-elastic variations of the telescope structure will induce a variation of the LoS of a given telescope with respect to the pointing direction of the fast telescope used as reference for the pointing. These variations will in turn induce additional and undesirable displacements of the stars, which have the same impact on the photometry as the kinematic differential aberration mentioned above.

**Jitter:** Variations of the satellite pointing direction induce short-term displacements of the stars (jitter). Hence, due to the fixed position of the mask, part of the flux coming from a star is lost. Additionally, part of the flux from a neighbouring parasite can enter the mask and pollute the photometry of the target. In either case, the flux of the target will be modulated by the coherent and incoherent variations of the pointing direction of the satellite.

**Outliers:** The occurrence of a cosmic ray or a glitch can perturb a light curve. Such perturbations can introduce important artefacts, in particular on the Fourier analysis. Hence, impacted measurements must be removed and replaced by a representative value of the star flux.

**Pixel saturation:** CCD pixels have a finite full well capacity and any charge beyond this capacity will spill into adjacent pixels of the same column (spillage into adjacent columns is prevented within the CCD). For the normal telescopes, the saturation limit is around magnitude 9.1. Therefore, stars brighter than these limits will be saturated. There is a strong scientific interest in the photometry of very bright, saturated stars; but since such stars have heavily distorted PSFs, they will require special photometry methods.

**Smearing (trailing):** After each integration, the CCD pixel data are read out. During this readout the CCD remains sensitive to the incident light and this produces the effect of smearing. The manifestation of this effect is that each star image has a uniformly bright “tail” along the columns, either in one or both directions depending upon the readout method chosen. The magnitude of this effect depends on the ratio of the readout time to the integration time.

**Sky background:** Deriving for each star the associated background flux is of major importance: not only for the analysis of the transit depth or the seismic analysis, but also for the photometry measurements based on weighted mask and for the photometric jitter correction. Indeed, an incorrect value for the background level decreases the efficiency of the weighted mask with respect to the confusion problem as well as the efficiency of the photometric jitter correction.

**Response function of the instrument:** The intensity of a given star will be different between the telescopes because the gain of the electronic chains, the quantum efficiency of the CDDs, and the differing aperture and transparency of the telescopes. Furthermore, crosstalks between different electronic chains are expected to occur and will introduce an absolute bias (offset) on the photometry measurements. Although the bias will be constant, it will nevertheless be different from one telescope to another. Therefore, before comparing and averaging (temporally and spatially) the light-curves associated with the same star but coming from different telescopes, it will be necessary to transform the digital signal into a signal that can be directly compared and averaged. This is why a correction of the global gain of the instrument (optical, CDD and electronic) as well the crosstalk patterns must be performed prior any comparison and averaging of the light-curves.
Long-term trend: The global gain of a telescope (see above) is expected to vary with the temperature. In addition to the variation of the global gain with the temperature, we will have a long-term decrease of the intensity because of the aging of the optics and of the CCD. All these variations are expected to occur at long time-scale (from weeks to several months) and must be corrected afterward on-ground.

4.11.1.2 OVERVIEW OF THE BASE LINE DATA PROCESSING ALGORITHMS

We present below the current base-line of the PLATO Data Processing Chain (DPC).

4.11.1.2.1 Photometry methods

**Weighted mask:** Instead of using a classical aperture (binary) mask, we will use a weighted mask derived from an adequate analytical function (e.g., a Gaussian). Such weighted mask can reduce the pollution induced by the presence of a parasite. Indeed, with such weighted mask, we can put more weight in the center of the star image and less weight in its tail.

**Mask update:** To prevent the star from going out of the mask due to the differential aberration we will update the mask positions frequently. Each mask update introduces a discontinuity. When a weighted mask is used, the more frequent the updates, the lower the impact of the discontinuities on the seismic analysis. In contrast, updating a classical aperture mask introduces important discontinuities whatever the frequency of the updates. This is the second advantage of the weighted mask compared to classical aperture mask. To minimize the discontinuity caused by each update, we will update the weighted mask as frequently as computational resources allow.

**Line Spread Function Fitting:** As an attractive alternative to aperture-based photometry, we are considering an additional photometric algorithm based on 1D fitting of the projection of the PSF on two perpendicular axes. This photometric method, referred to as Line Spread Function Fitting (LSFF), is only weakly sensitive to confusion, differential aberration and jitter. A description of the method and preliminary results showing that it is applicable to PLATO were presented in REF2 (see also and REF1). However, these results must be consolidated using the images computed with the PLATO simulator (PLATOSim) using realistic models of the PSF. We must also investigate whether or not it can be implemented on-board, given the performance of the on-board DPUs.

4.11.1.2.2 Light curve Correction

In order to get rid of the perturbations and problems mentioned in Section 4.11.1.1 different corrections must be applied to the light-curves. Among them, we emphasize the following:

**Photometric correction of the satellite jitter:** Jitter correction can be easily corrected as soon as we know accurately the PSF associated with a given target and the displacements of that target at each instant (see details in REF1 and REF3). Since the PSF, the mask and the star displacements differ from one telescope to another, the jitter correction is different from telescope to telescope. Since the light-curves from all individual telescopes will be downlinked, this correction can be done on-ground with methods that remain TBD.

**Outlier detection and rejection:** The flux of a star will be obtained by averaging (on-ground) intensity measurements originating from different telescopes. Furthermore, for the majority of the targets, the star intensity measured on a given telescope is time-averaged on-board in order to decrease the cadence of
the data. Before performing such averaging (in time and space), we will discard those measurements that depart significantly from a reference level. This reference level will be obtained on-board on the basis of the median and the standard deviation computed by considering the measurements from the different telescopes simultaneously monitoring the same star.

4.11.2 CONFIGURATION AND CALIBRATION

Before starting an observation sequence, several different calibration processes need to be applied, among them we emphasize the following:

PSF modelling: In order to compute the weighted mask or to perform a jitter correction, it is crucial to derive the PSF associated with each target. The PSF is expected to change along the field of view. It is also expected to depend on the star’s colour. It will obviously not be possible to derive the PSF associated with each of the (around) 125,000 stars directly. However, we will acquire (during the calibration mode) time series of imagettes for about 1,000 reference stars. From this set of imagettes, we think it will be possible to derive a model of the PSF. Then, in order to derive the PSF of the other stars, we will perform an interpolation of the PSF model on the location (X,Y) of the target and – if needed – on the colour (B-V) of the target.

Sky background modeling: Zodiacal stray-light is expected to be the major contributor to the background. This source is expected to vary on the long term (of the order of month). Since the momentum wheels will be unloaded approximately each week, we will use this as an opportunity to re-calibrate the background map. In terms of spatial distribution, the Zodiacal stray-light is also expected to vary at large scale-length. Accordingly, we can expect that such variation can be modelled using a functional form (e.g. a bivariate polynomial). The parameters of this functional form will be fitted during the configuration mode using several measurements of the background performed at different locations of a full image. Once the free parameters are adjusted, they will be used during the observation mode to derive the background associated with each target.

Accurate positions of the targets: We need to define a mask for around 125,000 stars. The calculation of a mask requires an accurate determination of the star position on the CCD. It is possible to derive the position of a given target on the CCD (X,Y) coordinates from its known position in the sky (right ascension: alpha; declination: delta). Indeed, as soon as we know the pointing direction of a given telescope, the optical distortion, the placement of the CCDs and the distortion of the CCD grid, it is possible to define a set of coordinate transforms that relates (alpha, delta) to (X,Y). Hence, using a catalog of stars and the matrices for the coordinate transforms, we can derive accurately the position of any target.

Before doing so, it is required to both determine the pointing direction of each telescope and calibrate the optical distortion and the distortion of the CCD grid. This will be possible thanks to the around 1,000 reference stars that will be observed during the configuration mode. Indeed, the observation of these reference stars will provide their accurate positions (Xr,Yr). Then, from their known positions on the sky (alpha_r, delta_r) and their known accurate position on the CCD (Xr,Yr) we finally derive the set of matrices associated with the coordinate transforms as well as the pointing direction of a given telescope.

4.11.3 DATA PROCESSING SYSTEM ARCHITECTURE

The PLATO data processing system is made up of an on-board segment and a ground segment.
Concerning the on-board segment, with 32 normal cameras working at the cadence of 25 seconds and 2 fast cameras working at the cadence of 2.5 seconds, the amount of raw data produced each day is close to 189 Terabits. This volume must be compared to the hundred of Gigabits which can be actually downloaded each day to the ground. It is clearly not possible to transmit the whole amount of raw data. The role of the on-board treatments will be to reduce by a factor of more than 1000 the flow rate by downlinking light curves, centroid curves and imagettes at the cadence required by the science. The data flow studies (see TM budget given in section 6.3 and in [APD7]) have shown that it is possible to individually download on ground the data from each camera. Such a possibility will reduce the complexity of the on-board treatments (no on-board averaging of the data and fewer corrections to be implemented on board).

The PLATO ground data centre (PDC), whose tasks are described in section 5.5, will be responsible for the main instrumental corrections and will produce calibrated light curves and calibrated centroid curves as level-1 products. The PDC will perform some a posteriori verification of the onboard processing. Feedback from PDC to the on-board processing will include updates of the mask determination procedures, of other photometry algorithm parameters, of star sample selection, etc.

The figure below gives a simplified overview of the PLATO data processing architecture at the system level:

4.11.4 PAYLOAD MODES

The mode breakdown of the payload is as follows:

- **OFF mode**: all the equipments of the payload are off.
- **ICU Initialisation**: the ICU initializes and establishes the communication with the SVM; ICU is not yet able to take control of the other payload equipments, so in this mode, the ICU is the only equipment of the payload that can be controlled and monitored.
• Stand-by and service mode: the ICU is able to manage the whole Payload. All payload management services can be performed except scientific processes. This mode is mainly used in the following cases:
  o Payload equipments switching on (except ICU switching on)
  o SW maintenance
  o Uploading star catalogue in ICU memory
  o Waiting in case of LoS loss (during antenna steering, wheel unloading or 90° rotation)

• Fine pointing initializing: the F-DPU acquires the guide stars and initializes the FGS filter. This mode is ran until the F-DPU is able to deliver FGS data to the SVM. If a coarse pointing mode is needed, it will be a sub mode of this mode. But the need of such a coarse mode is not yet assessed.

• Configuration for observation: the ICU sends the star catalogues to the DPU. The N-DPU and the F-DPU acquires the target stars and configures themselves for the observation. This mode is ran at the beginning of a new pointing and after each 90° rotation.

• Periodic calibration: the N-DPU and F-DPU processes the CCD images in order to update the focal plane geometry model, the PSF models, the background models and the masks. These processes are not compatible with the observations processes, so they are performed outside of the observation mode, typically before entering observation mode after wheel unloading.

• Observation mode: the N-DPU, the F-DPU and the ICU perform the scientific processes and produces science TM as described in the chapter on the observation mode (following chapter).

The chart below gives an overview of the transition between modes:
4.11.5 REQUIREMENTS IN OBSERVATION MODE

This section gives the high level data processing requirements associated to the observation mode. In the following requirements, the number of stars specified for each sample category is given per observation run and not for the entire mission duration.

Moreover, the cool dwarfs which are mentioned in the scientific requirements (sect. 3) belong to magnitude limited stellar populations totalling about 5 times more stars, because the cool dwarf fraction is about 20%. Dimensioning the data treatments to exactly the expected number of cool dwarfs in each sample implies a risk of mis-selection when choosing the stars to monitor, hence a decrease of the final number of useful targets. This is why the data treatment needs to be dimensioned for larger numbers of stars than specified in sect. 3.

Therefore the following numbers will be used for dimensioning the data treatments, resulting from trade-offs made at the level of the science team:

sample P1: cool dwarfs/subgiants with noise $\leq 34$ ppm/hr
  - total per pointing = 10600, with margin 50% = 15900
  - total per FPA = 6720, with margin 50% = 10080

sample P2: cool dwarfs/subgiants with mV $\leq 8$, >2 years
  - included in P1 sample

sample P3: cool dwarfs/subgiants with mV $\leq 8$, >2 months
  - included in P1 sample

sample P4: cool dwarfs/subgiants with noise $\leq 80$ ppm/hr
  - total per pointing = 167000, with margin 50% = 250500
  - total per FPA = 102200, with margin 50% = 153300

sample P5: cool/dwarfs/subgiants with mV $\leq 11$
  - included in P4 sample

All the figures given in the requirements below shall be the inputs for all the data processing dimensioning activities (hardware and software):

**Normal camera requirements:**

For sample P1:
  - Calculate and transmit individual camera intensities of 10080 stars every 50 sec.
  - Calculate and transmit individual camera centroids of 100 stars every 50 sec.
  - Calculate and transmit individual camera centroids of 9980 stars every 600 sec.
Acquire and transmit imagettes for n=2000 (max.) stars every 25 sec.

For sample P4:
- Calculate and transmit individual camera intensities of up to 151770 stars every 600 sec.
- Calculate and transmit individual camera intensities of up to 1530 stars every 50 sec.
- Calculate and transmit individual camera centroids of 1530 stars every 50 sec.

**Fast camera requirements:**
- Calculate and transmit individual camera intensities of 400 stars every 50 sec.
- Calculate and transmit individual camera centroids of up to 360 stars every 50 sec.
- Calculate and transmit individual camera centroids of up to 40 stars every 2.5 sec.
- Acquire and transmit imagettes for m=40 stars every 2.5 sec.
- Provide angle error measurements to SVM AOCS.

The parameters n and m (n = number of imagettes per normal telescopes; m = number of imagettes per fast telescope) will be maximized depending on the available downlink bandwidth and the final compression ratio. The TM budget shows that it could be possible, with a compression ratio of 2:0, to transmit up to 2000 imagettes per normal telescope.

### 4.11.6 ONBOARD DATA PROCESSING ARCHITECTURE

The PLATO payload Data Processing System (DPS) is made up of several DPUs connected to two ICUs working in cold redundancy (excepted the Router Units inside the ICUs which can work in hot redundancy) through a SpaceWire network. The ICUs are connected to the SVM through SpaceWire links.

There are 16 normal camera DPUs. Each normal camera DPU (N-DPU) is responsible for processing the data (sample P1, sample P4) of two normal cameras: each N-DPU is connected to two N-FEE. The processing cadence for normal DPUs is 25 sec.

There are 2 fast camera DPUs. Each fast camera DPU (F-DPU) is responsible for processing the data of one fast camera: each F-DPU is connected to one F-FEE. The processing cadence for fast DPUs is 2.5 sec.

In the observation mode, the main tasks of the DPUs are:
- To acquire and store full-frame images sent by the FEE (normal DPUs: one 4510x4510-pixel image / 6.25 sec per normal camera; fast DPUs: four 4510x2255-pixel images / 2.5 sec). At the FEE level, no pre-processing such as windowing is done. The full images corresponding to each CCD are transmitted entirely. The raw data acquired from the ADC are just serialized and sent to the each normal DPU through two SpaceWire links and to each fast DPU through 8 SpaceWire links.
- To extract the star windows (normal DPUs: ~ 2x163380 6x6-pixel windows / 25 sec; fast DPUs: ~400 7x7-pixel windows / 2.5 sec).
- To transmit the imagettes to the ICU.
• To correct data (smearing, offset, background, gain).
• To compute flux and centroids.
• To update the photometric masks and star positions at a cadence of about 5000 seconds to correct for differential kinematic aberration.
• To transmit computed flux and computed centroids to ICU at the acquisition cadence (25 sec. for normal DPUs and 2.5 sec. for fast DPUs).

The F-DPUs have a supplementary function: they are responsible for providing angle error measurements directly to the SVM AOCS.

In observation mode, the role of ICU is:

• To detect and remove outliers by comparing the N measurements from the N telescopes sharing the same LoS (N=8 or N=16 or N=32).
• To stack for each telescope the flux and centroids (only the selected data are stacked).
• To compute for each telescope the mean (and the standard deviation) of the stacked measurements (stacked flux and stacked centroids) at a cadence depending of the sample category (50 sec. or 600 sec.).
• To compress the data before transmitting them to SVM.

In “configuration for observation” mode, the DPUs are responsible for:

• Identifying the list and the raw positions of the reference stars.
• Computing a background model.
• Computing the accurate positions of the reference stars and the distortion matrix.
• Computing for each reference star the parameters of the PSF model.
• Identifying all the targets and deriving their accurate positions.
• Deriving the parameters of the PSF associated with all the targets.
• Computing the masks and the window positions of all targets.

The role of the ICU in “configuration for observation” mode is mainly to provide to the DPUs some configuration parameters (catalogue, etc.), to schedule the DPU tasks, to manage the data flow and to perform cross checking operations between data from telescopes of the same LoS.

The figure below gives an overview of the PLATO data processing system architecture and of the data flow rates. This chart focuses on the sharing of the main functions and the data flows. It is a simplified view of the hardware architecture and does not replace the one given in section “Digital electronics”: the SpaceWire routers are not shown and the DPU assembly boxes (MEU) are not drawn.
5. SUB SYSTEM DESIGN

5.1 TELESCOPE OPTICAL UNIT (TOU)

The study of the TOUs includes the optical and mechanical designs, the analysis of suitable glasses, compatible with radiation cumulated dose, and thermo-mechanical analysis. Moreover a straylight analysis and a study of baffling system have been carried out.

There is no difference in the TOU design for normal and fast telescopes, but the latter will include low-pass or high-pass filters under form of special coatings on an optical surface of the optical train.

5.1.1 TOU OPTICAL DESIGN

The following optical configuration is considered the starting baseline for the Definition Phase. It is the result of the studies carried out during the Assessment Phase and in the Pre-Definition Phase, and takes into account the updated technical requirements, mainly driven by the reduction of the number of cameras and the needs to maintain the TOU performances capable to satisfy the science requirements.
The general performances and parameters of the baseline optical configuration are reported in the following table:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spectral range</td>
<td>500 – 1000 nm</td>
</tr>
<tr>
<td>Entrance Pupil Diameter</td>
<td>120 mm</td>
</tr>
<tr>
<td>Working f/#</td>
<td>2.06 @ 700 nm</td>
</tr>
<tr>
<td>Field of View</td>
<td>1151.5 degree²</td>
</tr>
<tr>
<td>Image quality</td>
<td>90% Enclosed energy &lt; 2×2 pixel² over 1108.3 degree²</td>
</tr>
<tr>
<td>Maximum Field Distortion</td>
<td>5.043%</td>
</tr>
<tr>
<td>Plate scale</td>
<td>15 arcsec/pixel</td>
</tr>
<tr>
<td>Pixel size</td>
<td>18 microns</td>
</tr>
<tr>
<td>CCD format</td>
<td>4510×4510 (×4) pixel²</td>
</tr>
<tr>
<td>FPA size</td>
<td>164.36 mm (2 mm CCDs gap)</td>
</tr>
<tr>
<td>Working Temperature</td>
<td>-80°C (at telescope TRP)</td>
</tr>
<tr>
<td>Working Pressure</td>
<td>0 atm</td>
</tr>
</tbody>
</table>

The optical configuration consists of one window, placed at the entrance of the telescope, and 6 lenses. The first surface of the first lens contains an aspherical term (K, a⁴, a⁶), while the second surface has been imposed to be flat in order to facilitate the interferometric surface measure during the aspheric manufacturing. All the other lenses are standard spherical surfaces. The first surface of the third lens is the optical system stop and guarantees a real entrance pupil diameter of 120 mm. A layout of the design is shown in the following figure:
Baseline optical layout

And the lenses parameters are reported in the following table:

<table>
<thead>
<tr>
<th></th>
<th>R</th>
<th>Thickness</th>
<th>Glass</th>
<th>K</th>
<th>a⁴</th>
<th>a⁵</th>
<th>Shape</th>
<th>Diameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>window</td>
<td>S1</td>
<td>infinity</td>
<td>BK7G18</td>
<td></td>
<td></td>
<td></td>
<td>circular</td>
<td>190</td>
</tr>
<tr>
<td></td>
<td>S2</td>
<td>infinity</td>
<td>6.000</td>
<td></td>
<td></td>
<td></td>
<td>190</td>
<td></td>
</tr>
<tr>
<td>Lens 1</td>
<td>S3</td>
<td>177.857</td>
<td>23.000</td>
<td>S-FPL51</td>
<td>-3.681</td>
<td>3.605E-8</td>
<td>circular</td>
<td>178</td>
</tr>
<tr>
<td></td>
<td>S4</td>
<td>infinity</td>
<td>27.351</td>
<td></td>
<td></td>
<td></td>
<td>178</td>
<td></td>
</tr>
<tr>
<td>Lens 2</td>
<td>S5</td>
<td>795.855</td>
<td>7.000</td>
<td>N-KZFS11</td>
<td></td>
<td></td>
<td>circular</td>
<td>142</td>
</tr>
<tr>
<td></td>
<td>S6</td>
<td>135.943</td>
<td>56.975</td>
<td></td>
<td></td>
<td></td>
<td>142</td>
<td></td>
</tr>
<tr>
<td>Lens 3</td>
<td>S7</td>
<td>151.697</td>
<td>23.000</td>
<td>CAF2</td>
<td></td>
<td></td>
<td>circular</td>
<td>130</td>
</tr>
<tr>
<td></td>
<td>S8</td>
<td>-225.536</td>
<td>59.886</td>
<td></td>
<td></td>
<td></td>
<td>130</td>
<td></td>
</tr>
<tr>
<td>Lens 4</td>
<td>S9</td>
<td>-742.200</td>
<td>17.000</td>
<td>S-FPL53</td>
<td></td>
<td></td>
<td>circular</td>
<td>131</td>
</tr>
<tr>
<td></td>
<td>S10</td>
<td>-139.241</td>
<td>16.240</td>
<td></td>
<td></td>
<td></td>
<td>131</td>
<td></td>
</tr>
<tr>
<td>Lens 5</td>
<td>S11</td>
<td>-101.194</td>
<td>5.000</td>
<td>KZFSN5</td>
<td></td>
<td></td>
<td>circular</td>
<td>129.6</td>
</tr>
<tr>
<td></td>
<td>S12</td>
<td>-144.005</td>
<td>115.547</td>
<td></td>
<td></td>
<td></td>
<td>129.6</td>
<td></td>
</tr>
<tr>
<td>Lens 6</td>
<td>S13</td>
<td>-103.083</td>
<td>5.000</td>
<td>N-BK7</td>
<td></td>
<td></td>
<td>circular</td>
<td>154</td>
</tr>
<tr>
<td></td>
<td>S14</td>
<td>infinity</td>
<td>4.000</td>
<td></td>
<td></td>
<td></td>
<td>154</td>
<td></td>
</tr>
<tr>
<td>FPA</td>
<td>S15</td>
<td>infinity</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>square</td>
<td>184</td>
</tr>
</tbody>
</table>

The apertures of the lenses have been defined by setting a 7% vignetting factor at the edge field (having FPA coordinates 14.3 degree, 14.3 degree) and by over sizing the obtained aperture diameters by 2 mm (1 mm on aperture radius) to allow the lenses mounts. The last lens (the one in front of the FPA) has been cut in such a way to exploit only the part covered by FPA (avoiding vignetting) in order to reduce
the mass. With this assumption the overall mass due to the optical elements has been estimated to be about 5.0 Kg.

The polychromatic enclosed energy over the full Field of View is shown in the following figure. The weight of the wavelengths have been set by taking into account the detector quantum efficiency and the G0 reference star spectrum. Nevertheless, the performances are maintained also for a flat spectrum (i.e. all the wavelengths have the same weight). The polychromatic PSF at the different coordinates on the FPA in 4×4 pixel$^2$ are then shown.
Polychromatic PSFs at FPA coordinates (from top left to bottom right) 0,0 degrees, 0,2 degrees, 0,4 degrees, 0,6 degrees, 0,8 degrees, 0,10 degrees, 0,12 degrees, 0,17.7 degrees, 13.7, 13.7 degrees and 14.4, 14.3 degrees. Each box have size corresponding to 4x4 pixels.

The Field of View for which the optical configuration has been design has FPA coordinates 14.3 degree, 14.3 degree, while the corrected Field of View (90% EE < 2×2 pixel) has FPA coordinates 13.7 degree, 13.7 degree. A scheme is shown in figure below.

The estimated corrected Field of View area falling on the FPA is 1108.3 degree².
The insertion of the window as first optical element is due to multiple purposes:

1. It mitigates the thermal shock on the first lens.
2. It shields the S-FPL51 (moderate rad-hardened glass) from direct incoming high energy radiation, mainly solar protons (cf. 5.1.2)
3. It is foreseen a low emissivity coating in the IR deposited on the external window surface to reduce the axial thermal gradient along the TOU optical axis (TBC).
4. It reduces radial thermal gradient effects on the surface exposed to the space (been a plane parallel element the radial deformation has almost no effects on the optical quality).

All the surfaces are planned to be coated with antireflection in the wavelengths band 500-1000 nm. A pass band filter (coating) in the same wavelengths band is foreseen to be added to one of the lens surface (possibly on the STOP surface to avoid differential effects on the fields). The coatings definition will be studied during the Definition phase.

The aspherical surface on the S-FPL51 has a maximum deviation from the best fit sphere of about 1.050 mm. The sag of the aspheric surface, the sag of the best fit sphere and the relative deviation are shown in the figure below. The aspheric manufacturing process is under study in conjunction with the industries.
5.1.1.1 PRELIMINARY TOLERANCE ANALYSIS

The following are preliminary tolerance estimates of the elements for the TOU optics. It is based upon a MonteCarlo deterioration of the performances defined as a 80% EE< 2×2 pixel² over the corrected FoV. It does not include any compensator; in particular focus is removed as potential compensator, so these are to be assumed as “in-flight” tolerances. Lenses are numbered L1 to L6 starting from the front lens (the one looking at the sky) to the last lens (the one facing the detector).

The thickness lenses tolerance values have been estimated to be 30-50 micron. Tolerance on the stop positioning was estimated to be of the order of 10 micron.
We have also investigated the effects on the displacement of the image on the focal plane due to the optical elements tilt and/or decentring, obtaining, as shown in RD9, that this is of the order of 1.5 micron rms, a quantity significantly smaller than the displacement related to possible and unavoidable movements of the detector with respect to the TOU. We recall here, that any displacement in the focal plane can be treated to a large extent in the data reduction process.

5.1.2 OPTICAL MATERIAL ANALYSIS

Lens materials have been selected after a study of radiation effects on glass for an 8 years lifetime in L2 point (cf. RD3).

This study has concluded that the darkening of glass due to radiation environment in L2 only appears in the first millimetre of the first lens glass. For the others lenses, they are no more issue, because protected by the entrance window and by the telescope structure provided that this structure does not present important holes.

Moreover, the fluorescence due to the irradiation of the lenses is emitted in the UV band of the spectrum and hence it will be easily filtered out to avoid contamination in the focal plane.

As result of this study, radiation resistant well known glasses like BK7, BK7 G18 (rad-hardened version) or CaF2 can be used for the entrance optical part (lens or window). For the others lenses, more usual glasses can be used. The total transmission loss will be lower than 0.5 % per year in L2 point, for a front lens (or window) made in BK7.

For radiation aspect, the only possible candidates for the window are then CaF2 crystal, or BK7. Since CaF2 is considered as a very fragile glass, and supports with difficulty thermal shocks, it cannot be used in a front position.

Our baseline is then to use BK7 G18 for the entrance window of the optical train.

5.1.3 TELESCOPE MECHANICAL DESIGN

5.1.3.1 DESIGN CONCEPT

The use of materials with different coefficient of thermal expansion and the large temperature difference between integration and operation requires a design able to accommodate the dimensional changes of the assembled components without leading to mechanical stresses which could result in structure warping (loss of positioning accuracy) or even in structural failures, especially in the case of the brittle optical glasses. Flexible, quasi-isostatic mounts were therefore implemented at each mechanical interface:

- Lenses to lens mounts
- Lens mounts to TOU structure
- TOU structure to S/C optical bench
- Baffle to TOU structure

The machining tolerances of the mechanical components and of the lens-mount subassemblies can be corrected during integration by shimming. Therefore all elements directly bolted to the TOU structure, including the FPA, have a three-point attachment, whereby spherical washers are foreseen to minimize
mechanical stresses when the fasteners are torqued. At the S/C interface (bipods) shims and spherical washers are foreseen, as well.

From the thermal architecture point of view it is required that the heat dissipated by the CCDs has to be evacuated through the TOU structure and radiated into deep space by the baffle and the outer surface of the first lens. Since the gradients along the TOU need to be minimized the TOU structure has to be realized of a material with high thermal conductivity.

At the same time the use of a material with moderate CTE allows the optimisation of the section necessary to guarantee the required thermal conductance.

The following materials were chosen for the main mechanical components:

- **AlBeMet AM162** for the TOU structure [tube and L1 mount]. This material shows an outstanding combination of properties (high thermal conductivity and heat capacity, high Young’s modulus, low density, and moderate CTE) which makes it the ideal choice for the realization of thermally stable lightweight structures for optical assemblies. The CTE matches the glass used for L1 (S-FPL51) and allows a design with minimized thermo-elastic stresses. The major drawback of this powder metallurgical aluminium-beryllium alloy is the toxicity of its dust and fumes which requires demanding precautions during the machining processes.

- **Ti6Al4V** for the quasi-isostatic mounts [some of the lens mounts and bipods at the optical bench interface]. The combination of high strength and moderate Young’s modulus and CTE makes this titanium alloy an ideal material for the realization of flexible structures. The low thermal conductivity represents an advantage in the case of the interface at the S/C optical bench (minimization of parasitic heat fluxes) but is a drawback at the interfaces between lens mounts and TOU structure (gradients).

- **Dispal S232 and S225F** for the lens mounts 3 and 4. These powder metallurgical aluminium alloys show very good CTE match to the glasses used for lens 3 and 4 (CaF2 and S-PFL53), have good thermal conductivity, moderate young’s modulus and density.

- **AA7075 and AA6061** for the baffle [interface ring and baffle cone, respectively]. Low density, high thermal conductivity, as well as ease of manufacturing and coating (blackening and gold plating) were the main drivers during the trade-off. Furthermore for the less demanding quasi-isostatic interface with the TOU structure the low Young’s modulus and high strength of the 7075 alloy are sufficient.

In the table below, the mentioned properties of the six materials are summarized.

<table>
<thead>
<tr>
<th>Material</th>
<th>Density [g/cm³]</th>
<th>CTE [ppm]</th>
<th>E [GPa]</th>
<th>λ [W/m.K]</th>
<th>Rp0.2 [MPa]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti6Al4V-STA</td>
<td>4.45</td>
<td>8.6</td>
<td>114</td>
<td>7</td>
<td>&gt;890</td>
</tr>
<tr>
<td>AlBeMet AM162</td>
<td>2.07</td>
<td>13.9</td>
<td>193</td>
<td>210</td>
<td>&gt;280</td>
</tr>
<tr>
<td>AA7075-T6</td>
<td>2.81</td>
<td>23.6</td>
<td>72</td>
<td>&gt;155</td>
<td>&gt;435</td>
</tr>
<tr>
<td>AA6061-T6</td>
<td>2.72</td>
<td>24</td>
<td>72</td>
<td>&gt;170</td>
<td>&gt;240</td>
</tr>
<tr>
<td>Dispal S232</td>
<td>2.80</td>
<td>18-19</td>
<td>88</td>
<td>&gt;120</td>
<td>&gt;405</td>
</tr>
</tbody>
</table>
5.1.3.2 MECHANICAL DESIGN DESCRIPTION

The TOU main structure consists of a machined tube with all the interface planes, threads and holes necessary to mount the other components. Bolts are foreseen to allow reliable assembly and disassembly, especially during the shimming operations.

The lenses are pre-assembled in their mounts by gluing.

All the optics are then mounted and co-aligned into the tube.

The baffle is bolted at the top rim of the tube and carries the standoffs for the upper section of the MLI.

The CAD snapshots in the following figures show current design. Its overall dimensions are listed in the following table.

<table>
<thead>
<tr>
<th>Element</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tube length</td>
<td>277 mm</td>
</tr>
<tr>
<td>Tube diameter</td>
<td>215-285 mm</td>
</tr>
<tr>
<td>Tube thickness</td>
<td>1.7-2.5 mm</td>
</tr>
<tr>
<td>TOU overall diameter</td>
<td>ca. 450 mm</td>
</tr>
</tbody>
</table>

5.1.3.3 MASS BREAKDOWN

Mass drivers are:
- Size & mass of the optics elements
- Thermal aspects (min. wall thickness to keep gradients within limits).
- Size of the baffle (geometry)

The present **nominal mass** of the mechanical structure of each telescope optical unit is estimated to be about 4.2 kg.

5.1.3.4 DESIGN STATUS

The design activities were focused on the fulfilment of the thermal and thermo-mechanical (optics mounts stability) requirements and no FEM modelling was carried out yet to verify the mechanical requirements.
Anyway, since the structure sections and geometry are mainly driven by the above mentioned requirements no clear critical area with respect to materials strength and first eigen frequency could be identified. The following items will for sure require optimisation work:

- Bipods at the interface to the S/C optical bench: Isostaticity requirements (not yet available) and max. allowed thermal conductivity have to be verified and optimised against the strength and first eigen frequency requirements.
- Lens mounts: Optimization of the contact area at the glass surface. Optimization of the thermal conductivity.
- Eigen frequency and strength verification.

Snapshots of the TOU mechanical design
5.1.4 STRAYLIGHT ANALYSIS

During the Assessment phase we have developed a method to analyse the stray light performances of one TOU of the PLATO satellite. We report here on the results obtained taking into account:

- the modifications going on in the optical design of the TOUs
- the impact of different characteristics of the model, mainly surfaces micro-roughness and
dust deposition on the first lens.

Several simulations using different Zemax Non Sequential (NS) models of the TOU, each characterized by different properties in terms of scattering properties and structure were performed. Differences are in terms of:

- scattering properties of the structure (absorbing or 10% lambertian),
- lenses border properties (absorbing, normal or 10% lambertian),
- roughness of lenses (20 or 10 Å rms),
- dust deposition (CL300, CL400, or CL500) on the first lens,
- presence/absence of a baffles.
- coatings of lenses, FPA and front window

The simulations have been performed in 2 steps:

1. In ZEMAX: the NS models have been fed with a fixed power source creating a plane wavefront simulating a point-like source at infinite distance. This source has been moved so that the rays impinge on the frontal lens of the TOU from various directions, but only along the line of diagonal of the FoV (from 0° to 100° respect to the TOU optical axis), assuming in such a way a rotational symmetric system (symmetry broken in reality by the square shape of the detector). Two detectors have been defined: the first, of 100 micron side, collects the image of the source; the second simulates the TOU FPA and has its dimensions. For every position of the source the collected powers of the two detectors have been recorded; the difference between the powers gives us the ghost/stray energy (if the position of the source is out of the FoV, the power of the FPA detector is the ghost/stray power).

2. Once obtained the ghost/stray power as a function of the position of the source, these data have been used to multiply `photons map' representing how many photons/s impinge on the entrance pupil of the TOU coming from stars and zodiacal light. Summing up the contributions for all the directions and dividing by the number of pixels, the number of photons/pixel/s is calculated.

For some specific issues (ghost dimensions and intensities) some detailed studies have been performed (cfr RD3)

5.1.4.1 STRAYLIGHT PERFORMANCES

In the following figure the ghost/image power ratios versus the direction of the source in degrees, for different models are plotted. The 'ideal' one is a model in which the lenses have front and back surfaces coated with a 99% transmission coating, and all other surfaces totally absorbing. All the other models have structure with lambertian scattering profile (90% absorbing), lenses with 10 or 20 Å micro-roughness (rmsxx), and the first lens with a cleanliness level of 300, 400 or 500 (dust xxx).
**Ghost/image power ratios for some models**

And in the next table the values of ph/pixel/s obtained for some of the models considered are reported. The first one (99% border) is a model with an ideal absorbing structure, with no micro-roughness or dust on the lenses and with a 99% transmitting coating on all the surfaces of the lenses (front, back and side). The others are models with different micro-roughness expressed in Å and different cleanliness level (CL xxx) of the first lens. The last one is a model with an external baffle (all the other models do not consider any baffle). Separated contributions from ghost of field stars, straylight of out-of-FoV stars and straylight of out-of-FoV zodiacal light are reported.

<table>
<thead>
<tr>
<th>Model</th>
<th>In FoV Stars ph/pxl/s</th>
<th>Out FoV stars ph/pxl/s</th>
<th>Out FoV Zodiacal light ph/pxl/s</th>
<th>TOTAL ph/pxl/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>99% BORDER</td>
<td>0.33</td>
<td>10.2</td>
<td>42</td>
<td>52.5</td>
</tr>
<tr>
<td>RMS10G15 DUST 500</td>
<td>0.5</td>
<td>0.5</td>
<td>1.025</td>
<td>2.025</td>
</tr>
<tr>
<td>RMS10G15 DUST 400</td>
<td>0.35</td>
<td>0.475</td>
<td>0.925</td>
<td>1.75</td>
</tr>
<tr>
<td>RMS10G15 DUST 300</td>
<td>0.3</td>
<td>0.475</td>
<td>0.9</td>
<td>1.65</td>
</tr>
<tr>
<td>RMS20G18 DUST 500</td>
<td>1</td>
<td>0.6</td>
<td>1.1</td>
<td>2.7</td>
</tr>
<tr>
<td>BAFFLE (RMS10G15 DUST 300)</td>
<td>0.35</td>
<td>0.325</td>
<td>0.75</td>
<td>1.425</td>
</tr>
</tbody>
</table>

**Photo-electrons/px/s for various models**

Main results are:

- For quite all the models the results are within specs (<3 ph/pxl/s, while the requirement was ~<20 ph/pxl/s)
- The only system in which this does not happen is that called ‘99% border’, a system in which the borders are such that Total Internal Reflection is possible. This implies that for some specific positions out of FoV a great part (of the order of tenths) of the radiation impinging on the Entrance pupil can reach the detector. For all analyzed systems this has been avoided using for...
the borders of the lenses a 10% Lambertian scattering profile, simulating lenses with blackened borders.

- The presence or absence of a baffle does not change dramatically the behaviour of the system (for stars both in-FoV and Out-of_FoV and zodiacal light out-of-Fov); it can raise the level of stray light for the in-field sources, acting as a collector.

The analysis has repeatedly taken into account progress in the choice of coatings for the window, the FPA and the lens material, so to check if the system is still in the specs.

![Graph](image.png)

**Ghost/image power ratios for updated models**

In the figure above, the power ratio of ghost and image are presented for models with different coatings: a ‘normal’ one (1% reflectivity), an antireflection coating and two systems (IR and IRx2) in which the front window is treated with a coating aimed to reduce the infrared emissivity (cf. RD3). The FPA CCDs have always been considered as reflecting as 1-QE.

The plots show that out of FoV, the behaviour is similar to the previous, while the in FoV behaviour depends on the coating of the window. However the introduction of coating on the CCDs takes to the doubling of the values of the ratio, where the ratio itself is not influenced by the point-like ghosts introduced by the front window. So we can be confident that, in any case, the ph/pixl/s values will be in the specs (<20).

### 5.1.4.2 LOCALIZED FEATURES

The previously reported analysis concentrates on averaged quantities, i.e. the average photons count per pixel over the whole FPA plane.

Some considerations can be done anyway regarding more localized ghosts due to double reflections of TOU surfaces.

#### 5.1.4.2.1 Point-like Ghosts

The introduction of a flat window in front of the system has a main consequence in terms of generation of ghosts: the creation of a focused point-like ghost caused by the double reflection of the detector and
the window. These ghosts maybe easily confused with a real star. To quantify the effect, we created a NS Zemax Model in which this particular ghost was recorded by a Zemax detector “twin” of the detector centred on the image, but axis-symmetric wrt the optical axis of the TOU (from geometrical considerations the ghost will have this position); the intensity of the ghost has been so collected for different positions of the source in the FoV.

The results are the following:

- The ghost has a quasi-linearly decreasing intensity going form the center of the FoV towards the border, vanishing for vignetting effects for position angles greater than 7°

- The central intensity of the ghost will depend obviously on the coatings of the detector and of the front window, and on the spectral type of the source; results are summarized in the following plot, where the ratio of the intensity of the ghost on the real image vs the position of the source is plotted. AR is a standard antireflection coating, IR a coating designed to have a low emissivity in the infrared (for thermal reasons) and Irx2 an ‘optimized’ version of IR.

Finally these data have been used, together with a stellar density model [cfr. RD3 and references therein] to ‘count’ how many of these ghosts (per 1 mag bin) will be present in a ‘typical’ PLATO FoV, so to understand what will be the impact in terms of ‘false positives’. The results are shown in the figure below.
5.1.4.2.2 Extended ghosts

Being a 7 refractive elements optical system, there is the possibility that a PLATO TOU creates \((15 \times 14) / 2 = 105\) ghosts due to double reflections.

Two of those are the ‘point-like’ ghosts analysed in 5.1.4.2.1 due to the FPA CCDs and the front window. The double reflection due to the two surfaces of the front window, on the other side, will contribute directly to the image (at least at first order). All the other double reflections will create an extended ghost on the FPA. From the Zemax Baseline file some parameters of this ghost has been extracted, namely the position, the radius and the percentage of rays not vignette. These values have been obtained for several positions in the field (along the diagonal, every \(1^\circ\)). Our analysis shows that the smallest extended ghost will have an area of \(~8000\) pixel, and that the signal will be \(~10^7\) fainter than the image. Obviously these values will depend on the real coatings applied and on the source spectrum.

5.1.4.3 CONCLUSIONS

Here are main conclusions and a roadmap for future work:

- for all the models the number of photons per pixel per second due to stray light sources are in specs
- the main contributor to the stray light is the ghost formation from the border of the last lens
- the baffle presence has to be checked and evaluated carefully, because, even if not changing things in a radical way, its presence can lead to some pros (for out of field sources of straylight), to expenses of contra in FoV.

We notice that our current analysis is based on several simplifications / assumptions:

- the assumption of a totally symmetric system
- the use for the micro-roughness and dust analysis of models strictly valid only in monochromatic light
- the use of a 'dust' BSDF limited at forward scattering and its simplification and modelling using the ABg model
- the use of coating/ BSDF still largely theoretical: no really lambertian material exists, so as the existence of a 99% uniform coating for the lenses should be checked. Even the real coating data, used in some of our analyses, has to be checked/verified with manufacturers.

The biggest simplification is that the total of stray light / ghost could be simply divided by the number of pixel and so obtains an average photon number. To overcome this simplification, some studies have been carried out to analyse in greater deep the behaviour of the ghosts; these studies make us confidant that the PLATO TOU mat satisfy the requirements for straylight given in the spécification document. Hence, in the future, analyses should be carried out introducing / updating the following input/data:

- small updates of the optical design that will intervene in the future
- contacting / discussing with manufacturer to obtain their best estimate about coating, roughness, scattering properties of optical and mechanical elements
- update the mechanical structure to a more realistic system
place the TOU in a realistic satellite, so to evaluate if sunshield and mutual scattering can have an influence.

Evaluating in a more localized way, and not only in average, how straylight and ghosts will affect the FPA. Carry out a full simulation of a PLATO TOU star field.

5.1.5 BAFFLES

Each TOU unit will be provided with a baffle. The aim of this baffle has evolved during the study of the TOU: if at the beginning it was introduced mainly for optical reasons (straylight reduction), soon it became clear that, due to constraints of allowance and mass, it was impossible to create a baffle large enough to have a real effect on out-of-field astronomical sources of straylight (cfr. §5.1.4). Since then its role has become twofold:

- Reduction of straylight from satellite: the baffle will reduce the possible straylight coming from the satellite itself, mainly the rim of the sunshield and the others TOUs.

- Thermal homogenization: the presence of the baffle will allow an homogenization of the conditions for all the TOUs, e.g excluding a direct view of the external solar shield, no matter what is the position of the single TOU on the optical bench. So the thermal control of the different TOUs should be simplified.

5.1.5.1 DESIGN

The main drivers in the design of the baffle are:

- Mass reduction
- No vignetting of the FoV
- Interface with the TOU structure
- The 'overlapping fields' dispositions of the TOUs in payload
- Space allowances

The first point has lead to the adoption of Aluminium as baseline material. The precise kind of aluminium will be decided to match, at best, the TOU tube structure. Moreover, the baffle will be as simple as possible. So the baseline design will be a conical one, cut so not to intercept the light from the Sun and reinforced internally by 2 diaphragms. The cone will have a thickness of 0.8 mm.

The second point has led to the definition of the minimal aperture of the cone: 40°.
The interface with the TOU structure will be done with an interface ring bolted to the TOU structure with eleven bolts. This interface ring will have also another use: it will host the entrance window, that will be mounted to the structure with springs.

On the interface ring there will be also the stands for the MLI that will cover the TOU.

The cone and the ring will be joint by laser welding or by an equivalent way. It will not be bolted or mechanically fixed to reduce weight and complexity.

The overlapping field concept for the disposition of the TOUs on the Optical Bench carries to a complication: different kinds of baffles. The Normal TOUs will be split in 4 different groups each looking in a slightly different direction, displaced along the four semi-diagonal of the FoV of an angle of ~9°; the presence of the Fast TOUs, coaxial with the payload give us a total of 5 kind of baffles. The difference between the various baffles will be limited to the cut plane of the cone: the angle of this plane wrt the optical/mechanical Z axis, and the angle of the plane of symmetry of the resulting section of cone wrt the sides of the detector (or the reference frame of the TOU).

The last requirement led us to define the height of the baffle as the minimum possible.

### 5.1.5.2 PARAMETERS

In the following table the parameters needed to define the 5 kinds of baffles are reported.

<table>
<thead>
<tr>
<th>Type</th>
<th>Cut Angle</th>
<th>Rotation angle</th>
<th>H [mm]</th>
<th>N exemplars</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-1</td>
<td>37.03</td>
<td>9.05</td>
<td>117</td>
<td>8</td>
</tr>
<tr>
<td>N-2</td>
<td>24.3</td>
<td>14.2</td>
<td>92</td>
<td>8</td>
</tr>
<tr>
<td>N-3</td>
<td>24.3</td>
<td>-14.2</td>
<td>92</td>
<td>8</td>
</tr>
<tr>
<td>N-4</td>
<td>37.03</td>
<td>-9.05</td>
<td>117</td>
<td>8</td>
</tr>
<tr>
<td>F-5</td>
<td>30</td>
<td>0</td>
<td>100</td>
<td>2</td>
</tr>
</tbody>
</table>
H is taken along the TOU Z axis, from the bottom of the baffle cone to its intersection with the cone cutting plane (see figure below).

![Cut view of a baffle](image)

The rotation angle is the angle of which the cone is rotated along the optical axis wrt the TOU reference frame.

It is clear from the data that N-1 and N-4, as N-2 and N-3, are ‘twins’ configurations, different only in terms of rotation angle (symmetric).

The mass of the baffle will obviously vary according to the type, but always in range [600-700]g.

### 5.1.6 THERMAL ANALYSIS

The thermal analysis of the TOUs has been performed in order to obtain -90°C ±1.5°C of the TRP mean temperature with the heaters switched off. The TRP location has been considered in the tube at a distance of 244mm from the CCD (near L3).

The FEM software is ANSYS and the simplified model is composed about of 1000 nodes.

The three different configuration of the baffle lead to three different thermal model concerning the geometry (see baffle section). The configuration regarding the Fast TOU differs from the other two also for the heat generated from the CCD and dissipated through the tube of the TOU. These are called hereafter as 1&4, 2&3 and Fast. The height of the baffle is limited for the configuration 1&4 by geometrical constrains (lower limit). The height is considered as the distance of the front surface of the window with the center of the baffle (the intersection between the tilted cutting plane and the optical axis): it is impossible to reduce the height below 117mm because the cutting plane would intersect the supporting flange. For the configuration 2&3 the baffle has been dimensioned in order to obtain the temperature of the configuration 1&4. For the fast TOU the baffle is oversized to keep into account more margins. In any case it dissipates more heat and it is easier to reach the needed temperature.

After this first optimization, the height of the baffle is kept constant, as given in the table below:

<table>
<thead>
<tr>
<th>Baffle height [mm]</th>
<th>Fast</th>
<th>1&amp;4</th>
<th>2&amp;3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>100</td>
<td>117</td>
<td>92</td>
</tr>
</tbody>
</table>
From the thermal viewpoint the configuration 1&4 is the most critical because in this configuration the baffle works as radiator with the best efficiency (the view factor of the baffle to the sky is the greatest one). In order to reach -90°C the problem is to decrease the coupling from the FPA to the baffle in order to increase the temperature. With the baseline mechanical design and with the available environment input the TOU reach a temperature in the order of -110/-120 °C.

To decouple the FPA and the baffle different solutions are considered, but the possibilities are:

- Decrease the conductance of the connections between the baffle and the tube
- Decrease the emissivity of the inner surface of the baffle
- Changing the material of the baffle
- Changing the conductance of the bipods. This is a critical point because the second source of heat is the OB (it is at a higher temperature that -90°C); the preference is to keep decoupled as much as possible the TOU from the OB, but also with an insulating link between them it is possible to increase few degrees the TOU temperature tuning a little bit the conductance of the bipods.

The parameters adopted for the lenses are shown in optical design section in this document and the conductance of the tube-lenses connection has been calculated according the current mechanical design. The values given in the table below report the overall conductance keeping into account the three point connection between the mount of lens and the tube, the mount itself and the flexures between the lens and the mount.

<table>
<thead>
<tr>
<th>Conductance [W/K]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Window / baffle</td>
</tr>
<tr>
<td>Lens 1 / tube</td>
</tr>
<tr>
<td>Lens 2 / tube</td>
</tr>
<tr>
<td>Lens 3 / tube</td>
</tr>
<tr>
<td>Lens 4 / tube</td>
</tr>
<tr>
<td>Lens 5 / tube</td>
</tr>
<tr>
<td>Lens 6 / tube</td>
</tr>
</tbody>
</table>

The other fixed parameters are described in the table below. It has to be noted that the radiation from the CCD to the L6 has been neglected because the temperature of the CCD is not considered as a boundary condition. For this reason the temperature of the L6 is underestimated in these analyses.

The heat from the CCD evacuated through the tube by conduction has been applied on the lower edge of the tube and distributed all over the circumference of the tube.
Inner emissivity | 0.94

The current baseline is without the thermal low-emissivity filter on the window.

### 5.1.6.1 TOU 1&4

We present different solutions to obtain -90 °C at TRP ±1.5°C. The differences between each solution are shown in the table below:

<table>
<thead>
<tr>
<th>Solution #</th>
<th>Conductance baffle/tube [W/K]</th>
<th>Baffle emissivity</th>
<th>Baffle material</th>
<th>Low-em. Filter on window</th>
<th>TRP Window L1 L2 L3 L4 L5 L6 baffle tube</th>
</tr>
</thead>
<tbody>
<tr>
<td>1&amp;4_1</td>
<td>0.0074</td>
<td>0.94</td>
<td>Al</td>
<td>No</td>
<td>-91.4 -122.6 -95.1 -93.8 -91.8 -91.3 -135.9 -91.5</td>
</tr>
<tr>
<td>1&amp;4_2</td>
<td>2.9558</td>
<td>0.15</td>
<td>Al</td>
<td>No</td>
<td>-90.7 -112.5 -93.6 -92.3 -91.0 -90.6 -92.5 -90.9</td>
</tr>
<tr>
<td>1&amp;4_3</td>
<td>0.0148</td>
<td>0.94</td>
<td>Al</td>
<td>Yes</td>
<td>-90.7 -108.9 -93.4 -92.8 -91.0 -90.6 -131.6 -90.7</td>
</tr>
<tr>
<td>1&amp;4_4</td>
<td>0.0296</td>
<td>0.94</td>
<td>Ti</td>
<td>No</td>
<td>-91.4 -117.4 -94.7 -93.4 -91.7 -91.3 -130.1 -91.4</td>
</tr>
</tbody>
</table>

Even if the temperature at TRP was approximately -90°C the distribution of the temperature is different depend on the considered case. In the following tables, the median temperature of each component and the thermal gradient are reported. For example with the solution 1&4_1 the window has the lowest temperature even if the gradient inside it is less than 2 degrees. The maximum gradient inside one lens appears in the case 1&4_1 for L1: the maximum principal stress corresponding to that lens is about 2 MPa. This behavior for the lens 1 is due to the high conductance of the connection: in the current mechanical design the material of the mount is AlBeMet, the same material of the tube. For this reason flexures between them are not foreseen. The high conductivity of the AlBeMet leads to the high conductance shown in the table in the previous section. Changing this connection will be easy to reduce the gradient also for lens 1.

The presence of the thermal filter for the case 1&4_3 is modeled setting the emissivity of the outer surface of the window to 0.2.

<table>
<thead>
<tr>
<th>Solution #</th>
<th>TRP</th>
<th>Window</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
<th>L4</th>
<th>L5</th>
<th>L6</th>
<th>baffle</th>
<th>tube</th>
</tr>
</thead>
<tbody>
<tr>
<td>1&amp;4_1</td>
<td>-91.4</td>
<td>-122.6</td>
<td>-95.1</td>
<td>-93.8</td>
<td>-91.8</td>
<td>-91.3</td>
<td>-</td>
<td>-</td>
<td>-135.9</td>
<td>-91.5</td>
</tr>
<tr>
<td>1&amp;4_2</td>
<td>-90.7</td>
<td>-112.5</td>
<td>-93.6</td>
<td>-92.3</td>
<td>-91.0</td>
<td>-90.6</td>
<td>-</td>
<td>-</td>
<td>-92.5</td>
<td>-90.9</td>
</tr>
<tr>
<td>1&amp;4_3</td>
<td>-90.7</td>
<td>-108.9</td>
<td>-93.4</td>
<td>-92.8</td>
<td>-91.0</td>
<td>-90.6</td>
<td>-</td>
<td>-</td>
<td>-131.6</td>
<td>-90.7</td>
</tr>
<tr>
<td>1&amp;4_4</td>
<td>-91.4</td>
<td>-117.4</td>
<td>-94.7</td>
<td>-93.4</td>
<td>-91.7</td>
<td>-91.3</td>
<td>-</td>
<td>-</td>
<td>-130.1</td>
<td>-91.4</td>
</tr>
</tbody>
</table>

<p>| Thermal gradient (difference between maximum and minimum temperature [°C]) |
|---------------------------|---------------------------|---------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|</p>
<table>
<thead>
<tr>
<th>Solution #</th>
<th>TRP</th>
<th>Window</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
<th>L4</th>
<th>L5</th>
<th>L6</th>
<th>baffle</th>
<th>tube</th>
</tr>
</thead>
<tbody>
<tr>
<td>1&amp;4_1</td>
<td>-</td>
<td>1.57</td>
<td>4.42</td>
<td>0.09</td>
<td>0.02</td>
<td>0.41</td>
<td>0.29</td>
<td>0.4</td>
<td>2.53</td>
<td>1.56</td>
</tr>
<tr>
<td>1&amp;4_2</td>
<td>-</td>
<td>3.83</td>
<td>3.25</td>
<td>0.12</td>
<td>0.01</td>
<td>0.3</td>
<td>0.27</td>
<td>0.4</td>
<td>1.42</td>
<td>1.76</td>
</tr>
</tbody>
</table>
For case 1&4_1, the pictures below show the temperature for the TOU, the baffle and lens L1.

Temperature for the TOU, the baffle and lens 1

### 5.1.6.2 TOU 2&3

This configuration is less critical and only two cases are presented:

**Possible solutions to obtain -90 °C at TRP ±1.5°C**

<table>
<thead>
<tr>
<th>Solution #</th>
<th>Conductance baffle/tube [W/K]</th>
<th>Baffle emissivity</th>
<th>Baffle material</th>
<th>Low-em. Filter on window</th>
<th>Window L1 L2 L3 L4 L5 L6 baffle tube</th>
</tr>
</thead>
<tbody>
<tr>
<td>2&amp;3_1</td>
<td>0.0148</td>
<td>0.94</td>
<td>Al</td>
<td>No</td>
<td>TOU_04g.txt</td>
</tr>
<tr>
<td>2&amp;3_2</td>
<td>0.0296</td>
<td>0.94</td>
<td>Ti</td>
<td>No</td>
<td>TOU_04e.txt</td>
</tr>
</tbody>
</table>
5.1.6.3 FAST TOU

For the fast TOU the baseline is described in case FAST_1, while the case FAST_2 shows the effect of the heaters. The heaters are applied in the upper edge of the tube.

### Possible solutions to obtain -90 °C at TRP ±1.5°C

<table>
<thead>
<tr>
<th>Solution #</th>
<th>Conductance baffle/tube [W/K]</th>
<th>Baffle emissivity</th>
<th>Baffle material</th>
<th>Low-em. Filter on window</th>
<th>Heaters [W]</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAST_1</td>
<td>0.0296</td>
<td>0.94</td>
<td>Al</td>
<td>No</td>
<td>OFF</td>
</tr>
<tr>
<td>FAST_2</td>
<td>0.0296</td>
<td>0.94</td>
<td>Al</td>
<td>No</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Solution #</th>
<th>TRP</th>
<th>Window</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
<th>L4</th>
<th>L5</th>
<th>L6</th>
<th>baffle</th>
<th>tube</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAST_1</td>
<td>-99.9</td>
<td>-116.6</td>
<td>-93.4</td>
<td>-92.1</td>
<td>-90.2</td>
<td>-89.8</td>
<td>-90.6</td>
<td>-92.6</td>
<td>-120.4</td>
<td>-89.9</td>
</tr>
<tr>
<td>FAST_2</td>
<td>-77.2</td>
<td>-106.4</td>
<td>-81.3</td>
<td>-79.8</td>
<td>-77.6</td>
<td>-77.2</td>
<td>-78.2</td>
<td>-80.4</td>
<td>-111.7</td>
<td>-77.2</td>
</tr>
</tbody>
</table>

### Median Temperature [°C]

<table>
<thead>
<tr>
<th>Solution #</th>
<th>TRP</th>
<th>Window</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
<th>L4</th>
<th>L5</th>
<th>L6</th>
<th>baffle</th>
<th>tube</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAST_1</td>
<td>-99.9</td>
<td>-116.6</td>
<td>-93.4</td>
<td>-92.1</td>
<td>-90.2</td>
<td>-89.8</td>
<td>-90.6</td>
<td>-92.6</td>
<td>-120.4</td>
<td>-89.9</td>
</tr>
<tr>
<td>FAST_2</td>
<td>-77.2</td>
<td>-106.4</td>
<td>-81.3</td>
<td>-79.8</td>
<td>-77.6</td>
<td>-77.2</td>
<td>-78.2</td>
<td>-80.4</td>
<td>-111.7</td>
<td>-77.2</td>
</tr>
</tbody>
</table>

5.1.6.4 BAFFLE CONNECTION WITH THE TUBE

The main parameter that could be easily modified is the connection between the baffle and the tube. In the cases computed it has been changed from 0.0074 to 2.9558 W/K. The value of 2.9558 could be obtained with the current mechanical design by means of 12 flexural points in aluminum. The value of 0.0074 could be at the limit of the feasibility.

A preliminary evaluation of these conductance values can be seen with the example in the table below. To reach the lower values of conductance each joining point should be coupled to two insulating washers, like in the figure below.
Inputs parameters of the baffle – tube coupling

<table>
<thead>
<tr>
<th>Conductance baffle/tube</th>
<th>N° joining points</th>
<th>Joining material</th>
<th>Flexure size [mm] (length/height/minimu m thickness)</th>
<th>Washer - Size [mm] (ext./int._diameter/height)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0074</td>
<td>4</td>
<td>Ti</td>
<td>23/7/0.7</td>
<td>Yes (ceramic) – 10/6/10</td>
</tr>
<tr>
<td>0.0148</td>
<td>6</td>
<td>Ti</td>
<td>23/10/0.7</td>
<td>Yes (ceramic) – 10/6/8</td>
</tr>
<tr>
<td>0.0296</td>
<td>12</td>
<td>Al</td>
<td>23/10/0.7</td>
<td>Yes (ceramic) – 8/4/12</td>
</tr>
<tr>
<td>0.0296</td>
<td>6</td>
<td>Ti</td>
<td>23/10/0.7</td>
<td>No</td>
</tr>
<tr>
<td>2.9558</td>
<td>12</td>
<td>Al</td>
<td>18/10/0.7 (current mechanical design)</td>
<td>No</td>
</tr>
</tbody>
</table>

**Baffle – tube connection: each joining point should be coupled to two insulating washers**

### 5.1.6.5 THERMO ELASTIC ANALYSIS

The case 1&4_1 has been analyzed also from the thermo-elastic point of view in order to evaluate the displacement of the lenses. In the table below the vertical displacement and the maximum rotation of each lens is presented.

<table>
<thead>
<tr>
<th></th>
<th>Vertical displacement [mm]</th>
<th>Tilt [arcsec]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Window</td>
<td>-0.589</td>
<td>10.14</td>
</tr>
<tr>
<td>L1</td>
<td>-0.507</td>
<td>0.058</td>
</tr>
<tr>
<td>L2</td>
<td>-0.45</td>
<td>0.029</td>
</tr>
<tr>
<td>L3</td>
<td>-0.334</td>
<td>0.018</td>
</tr>
<tr>
<td>L4</td>
<td>-0.225</td>
<td>0.016</td>
</tr>
<tr>
<td>L5</td>
<td>-0.2</td>
<td>0</td>
</tr>
<tr>
<td>L6</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The tilt is due to the not axial-symmetry of the model for the shape of the baffle, but they are negligible for the optical performance.
5.2 FPA

5.2.1 DETECTOR

The PLATO detector is a CCD with two separately connected sections to allow full frame (FF) or frame transfer (FT) modes.

It is a back-illuminated, back-thinned device, non-inverted type (non-MPP). An antireflection (AR) coating is required on its sensitive surface for quantum efficiency increase.

Only one readout register with two outputs is required for both the FF and FT devices.

The electrical wirings for the powering, the command-control of the CCD and an external PT100 temperature sensor are grouped in a flexi-cable, which is directly connected on the associated FEE by a micro D connector.

5.2.1.1 DETECTORS FOR NORMAL CAMERAS

The main parameters required for the FF detector are summarised in the following table:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nominal value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size (µm)</td>
<td>18 x 18 (square)</td>
</tr>
<tr>
<td>Pixel format</td>
<td>4510 x 4510 (+TBD over clock dummy pixels)</td>
</tr>
<tr>
<td>CCD dimensions Image area</td>
<td>81.180 x 81.180 mm², 2 perpendicular sides buttable,</td>
</tr>
<tr>
<td>CCD flatness</td>
<td>better than 40 µm peak to valley</td>
</tr>
<tr>
<td>Readout</td>
<td>2 outputs at 4 Mpx/sec</td>
</tr>
<tr>
<td>Readout Noise</td>
<td>&lt; 28 electrons r.m.s. with a bandwidth of 8.0 MHz</td>
</tr>
<tr>
<td>Full Well Capacity</td>
<td>&gt; 900 ke-/px min., 1000 ke-/px typ.</td>
</tr>
<tr>
<td>PRNU</td>
<td>&lt; 3.0 % for λ ≤ 700 nm</td>
</tr>
<tr>
<td></td>
<td>&lt; 5.0 % for λ &gt; 700 nm</td>
</tr>
<tr>
<td>Full Frame Readout Time</td>
<td>&lt; 3.1 s</td>
</tr>
<tr>
<td>CCD Exposure Duration</td>
<td>&gt; 21.9 s</td>
</tr>
</tbody>
</table>

5.2.1.2 DETECTORS FOR FAST CAMERAS

The main parameters required for the FT detector are summarised in the following table:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Nominal value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size (µm)</td>
<td>18 x 18 (square)</td>
</tr>
<tr>
<td>Pixel format (total)</td>
<td>4510 x 4510 (+25 over clock dummy pixels)</td>
</tr>
<tr>
<td>Pixel format (image area)</td>
<td>4510 x 2255 (+25 over clock dummy pixels)</td>
</tr>
<tr>
<td>CCD dimensions Image area</td>
<td>81.180 x 40.590 mm², 2 perpendicular sides buttable,</td>
</tr>
<tr>
<td>CCD flatness</td>
<td>better than 40 µm peak to valley</td>
</tr>
<tr>
<td>Readout</td>
<td>2 outputs at 4 Mpx/sec</td>
</tr>
<tr>
<td>Readout Noise</td>
<td>&lt; 28 electrons r.m.s. with a bandwidth of 8.0 MHz</td>
</tr>
<tr>
<td>Full Well Capacity</td>
<td>&gt; 900 ke-/px min., 1000 ke-/px typ.</td>
</tr>
</tbody>
</table>
5.2.2 FPA DESCRIPTION

5.2.2.1 GENERAL

The FPA has to fulfil these main requirements:

- Support 4 CCDs in the accommodations (normal = left, fast = right) given below,
- The 4 CCDs shall be “co-planar” to define a mean sensitive plane with a good flatness.
- The FPA has the possibility to be adjusted in position (along \(Z_{\text{CAM}}\) and around camera transverse axes) by use of 3 shims located between FPA and telescope.
- The FPA shall be electrically isolated from the telescope.
- The thermal power (CCD electrical consumption and thermal leaks) shall be evacuated by the mechanical I/F with the telescope.
- The operating temperature of the detectors during the observation phase is specified as lower than -65°C.
- The FPA shall protect the detectors against parasitic light, and against radiations to limit the cumulated dose to 5 krad (TBC) at EOL.

These requirements have led to the following design of the FPA:

- Each of the 4 CCDs is mounted thanks to a quasi-static mount on a support plate,
• This support plate is attached to the telescope structure thanks to a stiff Interface Ring, made of the same material as the TOU (AlBeMet 162) so that there are no differential thermal contractions during cool-down or operation.

• The CCD packages are thermally connected to FPA-telescope I/F via flexible thermal straps.

• Each of the flexi-cables is mechanically fixed on the associated CCD package, close to the bonding with the CCD die.

Finally, the FPA is covered by a hood (not shown), to protect it from dust and light. This hood can support a local part (between the plane of CCD and the plane of last lens) used as radiation shield, especially for cameras located at the edge of the optical bench, and then, poorly protected by their neighbouring cameras.
The flexi-cables have a free length of ~80 mm (TBC) from the bottom of the FPA to the top of the FEE. The distance between FPA and FEE is limited to a nominal value of 65 mm to get slightly bended flexi-cables allowing small misalignments, displacements or rotations between them during AIT, launch...

### 5.2.2.2 INTERFACES

Interfaces with both TOU and CCD have been discussed and agreed with the respective groups.

#### 5.2.2.2.1 Mechanical

Mechanical interface with the TOU has been agreed as 3 M8 (TBC) mounting points at a diameter of 256 mm. The three mounting points will be fitted with spherical washers and shims in order to allow focus and tip/tilt adjustment without introducing stresses in the FPA.

Excerpt from PLATO FPA ICD (PLT/LDX/ICD/10100 1.0)

Mechanical interface with the CCD is by means of 3 Invar studs with shims, as shown in the following figure.
5.2.2.2 Thermal

Both CCD-FPA and TOU-FPA are joined by means of 3-points isostatic mounts. In both, shims are used to guarantee alignment. Heat conduction through an interface made of Invar and with several layers, working in vacuum, is difficult to predict. Contact conductance enhancers cannot be used at these high precision locating interfaces. In order to guarantee CCD thermal control, copper thermal straps are used.

Straps are joined to the CCD below the output registers, where heat is dissipated, so that heat does not spread to the image area. Indium sheet (TBC) is used at this interface as a contact conductance enhancer.

On the TOU, 4 flat areas are used to join the straps with the interposition of indium sheet (TBD) as a contact conductance enhancer.

Images of both interfaces can be seen below.
FPA Thermal Interfaces

5.2.2.2.3 Electrical Interface

The FPA is electrically isolated from the TOU. This is performed at two spots:

- On the FPA side of the TOU Thermal Strap, by means of isolating washers and isolating adhesive (Stycast 2850Ft **TBC**, see previous paragraph)

- The mechanical interface, by means of isolating washers and collars (see following figure)

FPA Electrical Isolation

CCDs are connected to the FEE by means of a flexi cable and a Glenair 51-way micro-D plug connector (according to PLATO-E2V-TRE-012 1.0). FPA grounding is performed through this interface (TBC).
5.2.3 FPA CRITICAL PERFORMANCE PREDICTION

Extensive analysis has been performed to guarantee PLATO FPA performances. A summary of the main parameters follows:

5.2.3.1 MASS

Mass has been considered the main design driver. Current FPA mass is 1550g for NORMAL and 1320g for FAST FPAs. The difference between both is only due to the different thermal straps mass. As shown in the following paragraph, the design is overstiff, so there is confidence in reducing this value even further in the future.

5.2.3.2 FIRST EIGEN FREQUENCY

First Eigen frequency of the FPA is predicted to be 439 Hz (see figure below for first mode shape). Requirement is 250 Hz for X&Y and 200 Hz for Z, so the design is clearly overstiff.

![FPA mode shapes (left, 1st eigenshape 439 Hz, right, 2nd eigenshape 473 Hz)](image)

5.2.3.3 STRENGTH

Quasistatic (100g), thermo-elastic (+35°C/-100°C) and Buckling strength analyses have been performed.

Maximum Stress occurs at the Flexures (AlBeMet) in quasistatic 100g load along X (see image below). Sensitive Area deformation is below 8 µm Peak to Valley, together with a translation below 84 µm.
Minimum Buckling load is above 1700g. All MoS are above 0 in both quasistatic and thermo-elastic load cases.

5.2.3.4 MEAN PLANE FLATNESS

A tolerance budget has been prepared in order to assess final Support Plane Flatness. Following contributions have been considered:

- FPA manufacturing tolerance flatness: < 22 µm Peak to Valley, which could be improved
- FPA Thermo-elastic deformation (with respect to the FPA-TOU interface): 8 µm Peak to Valley (see paragraph above)

Root Square Sum of these values is 23 µm PTV. FPA flatness manufacturing tolerance is being re-evaluated with help of the Mock-Up, even though it is not made of the same material.

5.2.3.5 CCD TEMPERATURE

A detailed Thermal Model has been built in order to assess Thermal Control performance.

Most up-to-date data for Flex conductance and CCD power has been used. Conservative assumptions have been used for contact conductance and material performances.

Given the good thermal connection between TOU and FPA, the CCD surface temperature closely follows TOU temperature, with differences below 5°C for NORMAL FPA and 7°C for FAST FPA. FEE temperature changes have little effect on CCD Temperature.

An image of the temperature distribution for the worst case FAST FPA can be found below.
Power balance is as follows:

<table>
<thead>
<tr>
<th>ITEM</th>
<th>DISSIPATION (W)</th>
<th>CONDUCTIVE FLUX (W)</th>
<th>RADIATIVE FLUX (W)</th>
<th>DISSIPATION (W)</th>
<th>CONDUCTIVE FLUX (W)</th>
<th>RADIATIVE FLUX (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCDs</td>
<td>0.55</td>
<td>-</td>
<td>-</td>
<td>0.8</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>FEE-FPA</td>
<td>-</td>
<td>0.56</td>
<td>-</td>
<td>-</td>
<td>0.56</td>
<td>-</td>
</tr>
<tr>
<td>FEE- MLI</td>
<td>-</td>
<td>-</td>
<td>0.37</td>
<td>-</td>
<td>-</td>
<td>0.37</td>
</tr>
<tr>
<td>FPA- TOU</td>
<td>-</td>
<td>-1.07</td>
<td>-0.23</td>
<td>-</td>
<td>-1.23</td>
<td>-0.27</td>
</tr>
<tr>
<td>CCDs- L6</td>
<td>-</td>
<td>-</td>
<td>-0.18</td>
<td>-</td>
<td>-</td>
<td>-0.23</td>
</tr>
<tr>
<td>BALANCE</td>
<td>0.55</td>
<td>-0.51</td>
<td>-0.04</td>
<td>0.8</td>
<td>-0.67</td>
<td>-0.13</td>
</tr>
</tbody>
</table>

5.2.4 FPA INTEGRATION PROCEDURE

Integration of the FPAs is extremely delicate. For this reason, an integration procedure has been envisaged to allow safe FPA assembly while guaranteeing assembly tolerances (see PLT/LDX/PRO/002 Issue 1.1). Integration will take place in class 100 environment (TBC). A time budget has been prepared in order to better estimate cleanliness conditions requirement.

In summary, an Integration jig has been designed to allow safe CCD handling. Active surface is facing downwards all the time to reduce dust contamination to a minimum.
The 4 CCDs are put together over a baseplate and aligned by means of dowel pins and shims. Then the CCD support Structure is assembled to the already aligned CCDs and nuts are tightened.

The assembly is then transferred to a pre-assembled FPA structure and aligned by means of a template. Thermal Straps are assembled.

All the steps described will be demonstrated during integration of the purposely-built Mock-Up, made of non-fight grade materials (see below).
5.2.5 FPA VERIFICATION PROCEDURE

Verification of FPA alignment is not easy, given the hard requirements and extended temperature range. A verification procedure has been prepared, that shows the process (PLT/LDX/PRO/001 1.1).

In short, a Zygo GPI XP/D in combination with a 12” Beam expander and a He-Ne Laser will be used.

A 3D image of the Sensitive Surface, together with reference surfaces, will be taken and post processed to obtain both in-plane dimensions (edges of CCD active surfaces) and out-of-plane (flatness of CCD surfaces). This process can be performed both at ambient and Thermal Vacuum conditions.

5.2.6 MATERIALS AND PROCESSES SUMMARY

Materials and processes have been selected following Space Standards. Following table contains a preliminary materials and processes list for PLATO FPA.

<table>
<thead>
<tr>
<th>ITEM</th>
<th>MATERIAL</th>
<th>PROCESS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCD Support Structure</td>
<td>AlBeMet162</td>
<td>MAP PU1 Black Paint</td>
</tr>
<tr>
<td>Stray Light Mask</td>
<td>AlBeMet162</td>
<td>MAP PU1 Black Paint</td>
</tr>
<tr>
<td>Interface Ring</td>
<td>AlBeMet162</td>
<td>MAP PU1 Black Paint</td>
</tr>
<tr>
<td>Thermal Straps</td>
<td>OFHC Copper</td>
<td>Tin plating (TBC)</td>
</tr>
<tr>
<td>Nuts</td>
<td>A4-70</td>
<td>Passivation (TBC)</td>
</tr>
<tr>
<td>Bolts</td>
<td>Ti6Al4V</td>
<td>-</td>
</tr>
<tr>
<td>Washers</td>
<td>A4-70</td>
<td>Passivation (TBC)</td>
</tr>
<tr>
<td>Disc Spring</td>
<td>AISI301</td>
<td>Passivation (TBC)</td>
</tr>
<tr>
<td>CCD Package</td>
<td>SiC</td>
<td>-</td>
</tr>
<tr>
<td>Interface Washers &amp; Shim</td>
<td>Invar36</td>
<td>-</td>
</tr>
<tr>
<td>FPA Shim</td>
<td>Invar36</td>
<td>-</td>
</tr>
<tr>
<td>Adhesives Stycast</td>
<td>2850FT</td>
<td>-</td>
</tr>
<tr>
<td>Isolating</td>
<td>Washers/collars</td>
<td>Ceramic TBD -</td>
</tr>
</tbody>
</table>
5.2.7 MOCK-UP STATUS

A Mock-Up, including both the FPA and integration MGSE, has been built in order to assess feasibility of integration (see following image).

This Mock-Up is being integrated at the time of writing this document in order to assess feasibility of integration procedure.

The Mock-Up is made of non-flight materials in order to allow quick procurement and manufacturing, and is therefore not suitable for thermal or mechanical tests. The main differences between the Mock-Up and the Flight designs are:

- CCDs (including packages) will be substituted by aluminium dummies. No CCD, flex, connector, PRT, etc will be fitted, only the Package.
- CCD Support Plate will be made of Aluminium 6082T6.
- Interface Ring will be made up of Aluminium 6082T6.
- Straps will be made of Copper (not necessarily OFHC).
- Straylight mask will be made of Aluminium 6082T6
• All fasteners will be made of stainless steel A2-70
• Interface washers and Shims will be made of Aluminium 6082T6
• Adhesives and interfillers may not be present

5.2.8 FPA MASS AND POWER

<table>
<thead>
<tr>
<th>Mass (kg)</th>
<th>Normal FPA</th>
<th>Fast FPA</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPA mass: CCDs, support plate, straps, bipods,</td>
<td>1.550</td>
<td>1.320</td>
</tr>
<tr>
<td>interface to telescope</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20% of uncertainties</td>
<td>0.310</td>
<td>0.264</td>
</tr>
<tr>
<td>Total, including 20% of uncertainties</td>
<td>1.860</td>
<td>1.584</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Normal FPA</th>
<th>Fast FPA</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPA power: CCDs dissipation</td>
<td>0.550</td>
<td>0.800</td>
</tr>
<tr>
<td>20% of uncertainties</td>
<td>0.110</td>
<td>0.16</td>
</tr>
<tr>
<td>Total, including 20% uncertainties</td>
<td>0.660</td>
<td>0.960</td>
</tr>
</tbody>
</table>

5.3 ELECTRONICS

5.3.1 NORMAL FEE

5.3.1.1 OVERVIEW OF N-FEE PURPOSE AND FUNCTIONS, CONSTRAINTS

The primary function of the N-FEE is to operate the 4 CCDs of a telescope, digitise the image data and transfer it to the DPU. An overall schematic diagram is shown in the next figure.
Schematic of 4 CCDs and an N-FEE

Next figure shows the timing of the CCD readouts. Each CCD has an integration time of ~22 s and a readout time of ~3 s. The readouts are staggered at equal intervals of the 25 s period. The readout and data transfer to DPU are arranged so that the readout of one CCD is finished before the next begins, in order to minimise crosstalk and interference effects.
5.3.1.2 N-FEE FUNCTIONS

The N-FEE is responsible for providing all the timings and bias voltages for driving the 4 E2V CCD-270 imagers, further, it is responsible for reading out the pixel data and digitising this data, then transferring it via SpaceWire to the DPU for further processing. The N-FEE also handles various housekeeping tasks, such as monitoring voltages and temperatures and passing these onto the DPU.

5.3.1.2.1 Overview of N-FEE blocks

The FPGA is the core of the N-FEE, this receives command packets from the DPU and timing and synchronisation data from the AEU. It generates all the clocks necessary for driving the 4 CCDs and drives the DACs responsible for providing the bias voltages.

Image data from the CCD is shifted down by the FPGA, then read out serially and potentially alternated through 2 separate ADCs. The digitised data from these ADCs is then read back into the FPGA where it is assembled into SpaceWire RMAP packets and transmitted to the DPU.

5.3.1.2.2 Bias supplies and clock drivers

Each of the 4 CCDs has an independent set of bias generators. Should a failure occur in one of the bias circuits or within a CCD the fault will not propagate to other CCDs in the camera.

The bias outputs are buffered and are generated as a multiple or division of a precision low-noise reference. The CCD output drain and reset drain voltages are programmable to a resolution of 12 bits. The dump drain voltage is a fixed fraction of, or equal to, the output drain voltage. The output gate voltage is a fixed fraction of the reference voltage.

The left and right output drains are independently buffered to eliminate crosstalk in the CCD output FETs which would otherwise originate from the finite output impedance and recovery time of the bias buffer after a bright star impulse. FETs in source follower connection have poor PSRR even at DC. The trade-off not to use the dummy outputs of the CCD saves power and removes the additive $\sqrt{2}$ broadband CCD noise, but places a lower noise constraint on the bias circuits.

Low noise components are used for the bias circuits, owing to the extreme sensitivity of the CCDs to bias noise. We have shown that noise of 0.1 LSB rms (in 14 bits) will be added to the CCD output signal due to a noise level of 8.76 µV rms on the output drain bias, in the band 800kHz – 20 MHz (centred about the 4 MHz readout frequency). The prototype N-FEE will verify that the required performance is met.

Circuit techniques and radiation tolerant components have been selected in order to achieve the required low noise performance. The selected components are the LTC RH1011S voltage reference, LTC RH1498 precision low noise op amp and LTC RH1078 micro-power op amp. Programming is performed via the Nat Semi DAC121S101QML 12-bit serial DAC.

Next figure shows the bias circuit for CCD1. There are four identical circuits.
Example bias supply circuit

The CCD clock drivers consist of a bank of Intersil ISL7457SRH quad CMOS drivers. The image clocks swing from 0V (SS) to 10V and the register clocks from 0.6V to 11V. As with the CCD bias, the noise on the clock levels must be extremely low, thus circuits similar to the bias supplies are used for the clock voltage regulation.

5.3.1.2.3 Analogue electronics: amplifier, CDS and performance (gain, noise...)

Next figure shows how pixels are digitised alternately by a pair of ADCs, each operating at 2 Mpix/s. The CCDs are read out in a cyclic sequence, one at a time. There is one pair of ADCs for the CCD left ports, one pair for the CCD right ports. A second mode of operation is also possible, where a single ADC digitises all consecutive pixels at 3 Mpix/s, whilst the other of each ADC pair is switched off.

An operational option which can save power, is to power down the video amplifiers and/or ADCs between CCD readouts. This option would be programmable within the FPGA. A warm-up time of about 1s would be allowed prior to each readout. This mode of operation and its effects on readout stability can be explored with the prototype N-FEE.
The overall gain of the video chain is derived from the peak star image signal from the CCD, with a 7.5 mA load (2.75k) on the output source. The peak output signal is in the region of 2V (700ke- to 900ke-, at 2.2 µV/e-). The video chain and ADC must rapidly recover from severe overloads, without phase reversal, from the effects of over-illumination. The overall voltage gain of the video chain is unity, and the differential ADC driver produces a +2V/-2V swing of 4.096V across the ADC input. The overall gain can be adjusted slightly as more is learned about the performance of the CCD.

The signal bandwidth is set at 5x the pixel rate, i.e. 20 MHz. This is higher than the 2x pixel rate for which e2V specifies CCD read noise. A trade-off of pixel-to-pixel memory vs. read noise is necessary. The use of 2-pole LCR filters improves settling time, and slight under-damping can be usefully employed.

The signal chain is designed to achieve better than 2 LSB rms of noise in 16 bits (0.5 LSB in 14 bits), a Pluto science requirement. An analysis of the total read noise has been performed and equates to 21.5 µV rms, or 0.7 LSB in 16 bits. This takes into account CCD bias noise, Johnson noise in bias resistors, amplifier Johnson and shot noise, KTC noise of the CDS circuit, CDS circuit efficiency, and ADC noise sources including quantisation noise, Johnson noise, sampling capacitor KTC noise, systematic noise and distortion.

A redundancy trade-off is achieved by having two video chains, one for the left ports of all CCDs of a telescope, and one chain for all the right ports. Each CCD is read out, in turn, from its left and right ports simultaneously, one CCD every 6.25 s over a 25 s cycle.

The requirements for selection of all components in the video chain are proven radiation tolerance, no phase inversion, extremely low noise and fast settling for 4 MHz performance to 16 bits. The amplifiers selected for the buffering and driving throughout the video chain are:

- **AD8021**: Ideal as an input buffer, amplifier and ADC driver, possibly the best fast 16-bit ADC driver on the market, and useful as a front-end amplifier. However, the circuit application as a CDS buffer for Kepler has been questioned [RD-2]. Key features: BJT input, 2.1 nV/√Hz input voltage noise, 2.1 pA/√Hz input current noise, 0.01% in 23 ns for a 1 V step, 50ns overload recovery, 6.7 mA supply current.

- An alternative for the CDS buffer is the **AD8065**. Key features: ‘FastFET’, FET input, input voltage noise 7 nV/√Hz (10 kHz), input current noise 0.6 fA/√Hz (10 kHz), 145 MHz bandwidth at G=+1, 180 V/µs slew
rate, settling to 0.1% in 55 ns, no phase reversal, 6.4 mA supply current. However the input noise of the AD8065 consumes 0.25 LSB (14-bits) of the video chain noise budget, so the design had been adapted to allow either the AD8065 or the AD8021 to be used as the CDS buffer, together with an active droop compensation circuit to minimise the effects of the BJT input bias current of the AD8021.

Each CCD port is connected to its source load resistor and buffered by a unity gain low noise amplifier before being multiplexed into the first stage amplifier, as shown in the next figure.

The CCD source load dissipates 155 mW and consists of three 1206 resistors in parallel, each dissipating 52 mW each. A connection is also made to the CCD substrate and dummy output. A small CM filter chokes any RFI which is coupled equally to the source signal and substrate reference. The connection from the CCD dummy output is connected to a wiring pad should it be needed as a fall-back option.

The DC coupling capacitor will remain charged to a fairly fixed level after power-on, so dielectric absorption is not an issue here, as it is in the CDS and filter circuits, where PPS film capacitors (or similar) are required to eliminate pixel-to-pixel memory effects. The coupling time constant is ~10 ms, which yields a droop error per pixel (reset to video) of 0.82 LSB in 16 bits.

A simple DC bleed bias and low leakage diode clamps peak excursion of the CCD signal to about +32V to prevent saturation of the AD8021 buffer amplifier. The amplifier is in single-ended connection with unity gain in order to maximise the SNR. The AD8021 buffer amplifier has an integral high impedance output switch which is used as the first stage of the input multiplexer. Combined with the second stage DG612 quad switch isolation of the CCD ports, in excess of 100 dB is achieved.

Next figure shows the multiplexer switch, CDS driver, LP filter, CDS circuit and FET buffer, and inverting stage. After the input multiplexer, a 2-pole low pass filter removes unwanted HF components originating from the CCD before the correlated double sampler (CDS) removes the reset noise associated with each pixel. An FET input amplifier with very low input bias current holds the reset level while the video level is AC coupled onto the input of the CDS buffer amp. An additional inverting stage feeds the 4 Mpix/s signal to a switch which multiplexes alternate pixels to the driver amps of one of two ADCs (or to one ADC in the 3 Mpix/s case). The additional inverting stage assures the correct signal polarity so that the driver amps have the necessary +2.048V offset for the ADC's AIN- input.
Schematic showing multiplexer of CCD left ports, pre-CDS row clamp, CDS driver, LP filter, CDS clamp and buffer, and signal inversion stage. Note the guarding of the high impedance paths against surface contamination leakage (much improved by conformal coating).

5.3.1.2.4 ADC: Description and performance (speed, power, noise, linearity etc.)

The ADC selected for the Plato N-FEE is the 16-bit AD7621. A batch of this PulSAR ADC was recently project-qualified for Gaia, and was found to have an SEL LET > 55.9 MeV.cm^2/mg. A batch will be LAT tested for Plato. The circuit configuration, including the AD8021 differential drivers, is shown in the next figure.
±1 LSB and DNL < 0.5 LSB in 16 bits. For a 100 kHz sine wave input, sampling at 3 MHz, the SNR is of the order of 88dB using the internal 2.048V reference and SINAD is 87.5 dB. We can expect related performance with a CCD waveform at 3 Mpix/s, i.e. an ENOB of 14.6 bits, and noise of ~1.4 bits rms.

Combining ADC noise of 1.4 LSB rms with the video chain noise of 0.7 LSB, we obtain 1.56 LSB rms, leaving a margin of 1.25 LSB rms (2 LSB rms total) for the rms combined effects of noise from the CCD bias and clock driver high level voltage, systematic noise from the power converter in the AEU, and EMC effects coupled into the power harness, CCD, etc.

The device has a power-down mode, and its parallel data output can be conveniently tri-stated for bus handling. An on-chip temperature monitor is included.

5.3.1.2.5 FPGA

The FPGA is implemented in Actel RTAX silicon

**FPGA block diagram**

The main interface to the DPU is through the SpaceWire Transceiver & Wishbone Controller. This receives SpaceWire packets from the DPU and transmits SpaceWire packets to the DPU and is then responsible for disseminating this data throughout the rest of the FPGA.

The control registers are used to record operational modes, bias voltages etc. sent from the DPU and hence control the operation of the FEE

CCD Timing Generation & Mode Control generates the vertical and horizontal shift clocks used by the CCDs and also defines whether we use the split readout option or not.

Image Acquisition is responsible for driving the CCD MUXs and ADCs and accepting the digitised pixel data from the ADCs.

SpaceWire RAMP Packet Builder takes pixel data from the Image Acquisition section and builds it into RAMP compliant packets which are then transferred back to the SpaceWire Transceiver & Wishbone Controller for transmission to the DPU.
SPI Interface & Housekeeping Control connects to the various DACs and ADCs on the N-FEE and sets up bias voltages etc. and reads back voltage and temperature information.

### 5.3.1.2.6 Data transfer: SpaceWire/Commanding

The interface between N-FEE and N-DPU is two SpaceWire links (notionally called SpW0 and SpW1). Control of N-FEE (accepting commands, responding to those commands, reading of housekeeping etc.) is carried out on SpW0 only.

The protocol used is RAMP in all cases, but the command interface is actually simulated RMAP with control registers and HK data etc. memory mapped for simple access.

Science data is not provided when the N-FEE is in the stopped state, or self-test state, but when running, science data is generated autonomously and RMAP packets are generated from the N-FEE and written to the N-DPU.

Science data may be driven over SpW0 only or both SpW0 and SpW1, depending on the operational mode of the N-FEE.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Split Readout</th>
<th>Num ADCs</th>
<th>Ping-Pong</th>
<th>Data Rate</th>
<th>SpW0</th>
<th>SpW1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>YES</td>
<td>2 x 2</td>
<td>NO</td>
<td>4MSPS</td>
<td>Left CCD</td>
<td>Right CCD</td>
</tr>
<tr>
<td>1</td>
<td>YES</td>
<td>2 x 1</td>
<td>NO</td>
<td>3MSPS</td>
<td>Left CCD</td>
<td>Right CCD</td>
</tr>
<tr>
<td>2</td>
<td>YES</td>
<td>2 x 2</td>
<td>YES</td>
<td>4MSPS</td>
<td>Left CCD</td>
<td>Right CCD</td>
</tr>
<tr>
<td>3</td>
<td>NO</td>
<td>2</td>
<td>NO</td>
<td>4MSPS</td>
<td>Odd Pix</td>
<td>Even Pix</td>
</tr>
<tr>
<td>4</td>
<td>NO</td>
<td>2</td>
<td>NO</td>
<td>4MSPS</td>
<td>Odd Pix</td>
<td>Even Pix</td>
</tr>
<tr>
<td>5</td>
<td>NO</td>
<td>1</td>
<td>NO</td>
<td>3MSPS</td>
<td>All Pix</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>NO</td>
<td>2</td>
<td>YES</td>
<td>4MSPS</td>
<td>Odd Pix</td>
<td>Even Pix</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note that modes 3 & 7 above, whilst technically selectable do not provide meaningful data as they are trying to ping-pong data through a single ADC.

End of image transfer is indicated by the transmission of a specially modified time packet which causes an interrupt in the DPU.

### 5.3.1.2.7 Housekeeping: Temperature monitors etc.

The N-FEE has internal housekeeping monitors and high and low resolution temperature monitors. All high resolution temperature monitors cover the range -90°C to +60°C (TBC) range to 16 bits. This eliminates the need to calibrate each range and zero the associated offsets and drifts. Only one zero operation is required for the entire range.

**5.3.1.2.7.1 High resolution channels (16-bit) for temperature monitors**

A total 8x PT100 sensors with 4.8 mK resolution (16-bit): 2x FPA, 2x baffle-telescope I/F, 4x CCDs. A 1mA current is applied at time of measurement of each TRP, dissipation ~64uW at -90°C. This prevents
prolonged invasive heating. The connection to each TRP is 2-wire, and 4-wire Kelvin connection within the N-FEE.

An example of the high resolution TRP monitor circuit is shown in the following figure. The DG612 switch has very low off-leakage (<0.25 nA) and is a good candidate for precision data acquisition. A stable reference voltage drives a bilateral current source. Each PT100 sensor is selected in turn for application of current and voltage measurement. The instrumentation amplifier is zeroed prior to each measurement (or series of measurements) of a sensor. The output voltage is fed to one of the 16-bit video ADCs, e.g. right port A-pixel (TBC). Each sensor is measured once per 25 s cycle (TBC), during the ‘dead times’ when the CCDs are not being read out. A double isolation switch (for fault tolerance) feeds the signal to the ADC.

5.3.1.2.7.2 Standard resolution (12-bit) channels for temperature and voltage monitors

Up to 16 standard resolution PRTs can be serviced, e.g. further sensors at the i/f with the camera support, on the baffle, at the FPGA within the N-FEE. It is expected that a maximum of 10 will actually be used.

The circuits for these are similar to the high resolution channels, except that MC14051 8-channel multiplexers are used to route the currents and read the voltages. The leakage performance of the rad hard variants from STM is an order of magnitude higher than the DG612, but adequate. For flight, the multiplexers could be replaced with devices from Aeroflex, e.g. from the RH5920 or UT16MX110MUX families.

There is also a temperature monitor output from each ADC. These are also monitored with 12-bit resolution.

The voltage monitors include: 12x CCD programmable bias for each CCD (VOD-L, VOD-R, VRD); 18x Raw secondary power input and regulated supply voltage monitors.

A bank of 8-channel multiplexed ADCs is used for the 12-bit channels. The ADC128S102QML from Nat Semi has been selected. The 12-bit ADCs can be read at any time, preferably between the CCD readouts, independently of the high resolution channels.

5.3.1.2.8 AEU Interface and power filter card

The AEU interface consists of a digital interface and a secondary power interface from the PSU.
5.3.1.2.8.1 Digital interface

50 MHZ (TBC) clock, which is routed to all N-FEEs in order to maintain synchronisation.

Synch signal, as shown schematically in figure of section 5.3.1.1, one pulse per 6.25 s, with the pulse extended every 25 s.

5.3.1.2.8.2 Power interface

The AEU PSU provides 6 secondary power lines to the filter card in the N_FEE. Each has a feed and return line.

5.3.1.2.8.3 Power filter card

In addition to CM filters within the N-AEU PSU, remote filters are required at the power input to the N-FEE in order to achieve the low noise performance of the camera. The N-FEE CM filters are supplementary to and do not replace the CM filters within the PSU.

The N-FEE filters must have a low impedance bond to the s/c structure, as their purpose is to shunt CM currents to the structure and thus prevent them from flowing across the sensitive CCD or analogue readout electronics. Interfering CM currents emanate not only from the switching of the DC-DC converter, but also from EMI induced in the long cables between the PSU and the N-FEE.

This approach requires that the s/c structure has a very low impedance, which is in conflict with the properties of a composite structure, e.g. SiC. Thus the requirement of low structure impedance must be addressed in order for the long harness scheme to work.

Simulations of a suitable filter, such as shown in following figures, predict an attenuation of around 70 dB for a typical converter frequency of 60 kHz, rising to 40 dB at 1 MHz. For analysis with CM signals, one half of the circuit was simulated, using the CM value of inductance to validate the simplified model. The CM chokes and capacitors are modelled with ideal elements, with their ESRs represented by ideal resistances.

At 60 kHz (typ. DC-DC converter frequency), the attenuation is 70 dB, rising from 60 dB at 100 kHz to 40 dB at 1 MHz. There is a singularity at ~70 kHz, which is a function of the bonding impedance (100 mOhm).
Simulation using ideal components and representative resistive losses

5.3.1.2.9 Grounding scheme

Grounding scheme
5.3.1.3 RESOURCES, ENVIRONMENT

5.3.1.3.1 Mechanical: Mass, volume, connector locations

CAD drawing of box showing PCBs, connectors

<table>
<thead>
<tr>
<th></th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/o protrusions</td>
<td>185</td>
<td>193</td>
<td>64</td>
</tr>
<tr>
<td>With protrusions</td>
<td>225</td>
<td>-</td>
<td>70.07</td>
</tr>
</tbody>
</table>

N-FEE box dimensions

5.3.1.3.2 Power

The voltage, current and power figures given in this section are requirements for the AEU. The figures take into account the following two points:
1. Voltages are specified at the output of the N-AEU PSU. A voltage drop of 0.5V is budgeted for the resistive loss in the combined go and return in the wiring from the PSU to the N-FEE, a length of up to 5m. An exception to this is the pair of wires for VDIG_SpW which must have a resistive loss in the combined go and return of no more than 0.2V for a load current of 50 mA.

2. The N-FEE can save power by switching on the video amps and ADCs as required. Some outputs will be on nominal load at all times (VCCD, VDIG). The load on other outputs (VCLK, VAN1, VAN2, VAN3_NEG) will reduce to as little as 4% of full load over a 6.25 s cycle period, i.e. full load for ~4 s and reduced load for ~2.25 s.

Two sets of figures for voltage, current and power are given below, each set showing BOL and EOL estimates. First following table shows the worst case where all circuits are powered continuously in order to achieve the required performance, whilst the second shows the case where the ADCs and video op amps are powered on/off in each 6.25 s cycle, provided this can be achieved without performance degradation of the N-FEE. The EID-B power budget for the combined N-FPA (CCD) and N-FEE is 7W +/-20%.

| Voltage and current at PSU output if all circuits are powered continuously |
|---|---|---|---|---|---|---|
| VCCD | VCLK | VAN1 | VAN2 | VAN3_NEG | VDIG_FPGA + VDIG_SpW | Ptot |
| +32.2V | +12.2V | +6.2V | -3.7V | -6.2V | +3.9V | +0.25 -0 |

<table>
<thead>
<tr>
<th>BOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak currents (mA)</td>
</tr>
<tr>
<td>Mean power (mW) in N-FEE and cables</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>EOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak currents (mA)</td>
</tr>
<tr>
<td>Mean power (mW) in N-FEE and cables</td>
</tr>
</tbody>
</table>

| Voltages and currents at PSU output if the ADCs and video op amps can be powered on/off over a 6.25 s cycle without performance degradation of the N-FEE |
|---|---|---|---|---|---|---|
| VCCD | VCLK | VAN1 | VAN2 | VAN3_NEG | VDIG_FPGA + VDIG_SpW | Ptot |
| +32.2V | +12.2V | +6.2V | -3.7V | -6.2V | +3.9V | +0.25 -0 |

<table>
<thead>
<tr>
<th>BOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak currents mA</td>
</tr>
<tr>
<td>Mean power mW in N-FEE and cables</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>EOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak currents mA</td>
</tr>
<tr>
<td>Mean power mW in N-FEE and cables</td>
</tr>
</tbody>
</table>
5.3.1.4 COMMONALITY WITH F-FEE

Some aspects of the FEE are common or similar for N-FEE and F-FEE, for example, the pixel rate is identical. Other aspects are significantly different, e.g. the F-FEEs are frame transfer devices and have a much shorter integration time, resulting in a much higher data rate, requiring eight parallel SpW links per telescope. Close co-operation between the N-FEE and F-FEE teams ensures minimum duplication of effort and sharing of expertise.

Aspects which are (predominantly) shared are: commanding, CCD bias supplies, clock waveforms, housekeeping.

Aspects which are significantly different are: FPGA and programming, number of SpaceWire interfaces and data rate.

5.3.2 FAST FEE

5.3.2.1 INTRODUCTION

The Fast FEE along with the Fast Focal Plane Assembly (F-FPA) and the Telescope Optical Unit (TOU) constitutes the fast camera. Two of these cameras are mounted on the Optical Bench (OB) as the 32 normal cameras. Fast cameras are interfacing with the Fast Electronic Unit (FEU) for control and data processing purpose. Fast cameras are interfacing with Fast Ancillary Electronic Unit (F-AEU) for power supplying and synchronisation purpose.

Due to the use of identical CCD detectors N-FEE and F-FEE have many similarities. Fast FEE differs by the fact that the 4 CCDs are read out simultaneously: the 4 frame transfers are then synchronous, every 2.5 seconds. Additionally due to less critical noise requirement the F-FEE uses an integrated analog front-end (AFE) electronics for, LM98640 from National Semiconductor, while the N-FEE uses a non-integrated 16-bit AFE. As for normal FEE, synchronisation of the two cameras is ensured by receiving from the associated F-AEU a high frequency signal (50 MHz) and a signal giving the information of 2.5 sec period beginning, also synchronised with the 25.0 sec period of the normal cameras.

5.3.2.2 FUNCTIONAL REQUIREMENTS

The functional requirements for a F-FEE are summarised in the next table.

<table>
<thead>
<tr>
<th>ID</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFEE-F010</td>
<td>Command handling: to receive / decode / execute immediate commands from FEU</td>
</tr>
<tr>
<td>FFEE-F020</td>
<td>Telemetry handling: to transmit detector digitized readout formatted into frames including time codes</td>
</tr>
<tr>
<td>FFEE-F030</td>
<td>Telemetry handling: to transmit housekeeping parameter frames to the FEU</td>
</tr>
<tr>
<td>FFEE-F040</td>
<td>HK collection: to acquire internal analog housekeeping (voltage, temperature, …) to achieve internal observability of the hardware functions</td>
</tr>
<tr>
<td>FFEE-F050</td>
<td>HK collection: to acquire external analog housekeeping (temperature) from F-FPA and TOU</td>
</tr>
</tbody>
</table>
FFEE-F060  To implement 8x SpaceWire link for interfacing with the FEU
FFEE-F070  CCD readout: to generate the detector readout sequence in frame – transfer mode
FFEE-F080  CCD readout: to process detector output analog signals up to digitisation including ‘extra pixels’
FFEE-F090  CCD readout: to provide the detectors with either fixed or adjustable bias voltages
FFEE-F100  CCD readout: to provide the detectors with either fixed or adjustable (high level only) clock signals
FFEE-F110  To synchronise detector readout sequence with external synchronisation signal
FFEE-F120  To synchronise detector readout clocks with external clock signal
FFEE-F130  Power supply: to filter and post regulate the incoming secondary voltages in order to guaranty unit performances

The functional design of a F-FEE is illustrated in the next figure.

![Functional Diagram](image)

### Functional Diagram

#### 5.3.2.3 PERFORMANCE REQUIREMENTS

Performance requirement of the unit are driven by the instrument performance requirement and the detector requirement as well. The main performance requirements for the F-FEE are summarised in the next table.

#### 5.3.2.3.1 Analog processing (F080)

<table>
<thead>
<tr>
<th>ID</th>
<th>Requirement</th>
<th>Value / range</th>
</tr>
</thead>
</table>

5.3.2.3.2 Detector readout (F070-090-100)

<table>
<thead>
<tr>
<th>ID</th>
<th>Requirement</th>
<th>Value / range</th>
</tr>
</thead>
<tbody>
<tr>
<td>FFE-P100</td>
<td>Clock level accuracy</td>
<td>&lt; 100 mV</td>
</tr>
<tr>
<td>FFE-P110</td>
<td>Clock level long term stability</td>
<td>&lt; 10 mV / K</td>
</tr>
<tr>
<td>FFE-P120</td>
<td>Bias accuracy</td>
<td>&lt; 20 mV</td>
</tr>
<tr>
<td>FFE-P130</td>
<td>Bias high frequency noise</td>
<td>&lt; 30 μV</td>
</tr>
<tr>
<td>FFE-P140</td>
<td>Bias long term stability</td>
<td>&lt; 3 mV / K</td>
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<tr>
<td>FFE-P150</td>
<td>Bias on flight trimming resolution</td>
<td>&lt; 5 mV</td>
</tr>
<tr>
<td>FFE-P160</td>
<td>Detector readout time</td>
<td>~ 1.5 s</td>
</tr>
<tr>
<td>FFE-P170</td>
<td>Detector integration time</td>
<td>~ 2.3 s</td>
</tr>
<tr>
<td>FFE-P180</td>
<td>Line transfer time</td>
<td>90 μs</td>
</tr>
<tr>
<td>FFE-P190</td>
<td>Vertical phase raise/fall time</td>
<td>22.5 μs</td>
</tr>
<tr>
<td>FFE-P200</td>
<td>Register clock period</td>
<td>250 ns</td>
</tr>
<tr>
<td>FFE-P210</td>
<td>Register clock rise/fall time</td>
<td>15 ns</td>
</tr>
</tbody>
</table>

5.3.2.4 INTERNAL DESIGN

5.3.2.4.1 Electrical Design

As depicted by the next figure, the F-FEE hardware is based on 4 main blocks:

- Analog electronics: encompasses the 8x analog processing chain based on the 14-bit LM98640 integrated AFE from National Semiconductor – the bias generator based on high stability voltage reference / high stability D to A converters / low noise amplifier and low pass filters – the clock translator
based on high stability voltage reference / high stability D to A converters / high current amplifiers / high speed high current clock drivers / dumping resistors.

Note: each detector is driven by a dedicated set of bias generators and clock drivers. Therefore each F-FEE unit hosts 4 sets of these functions.

Electrical Architecture

- Digital electronics: encompasses the programmable 40-MHz (TBC) clock sequencer – the command decoder in charge of the distribution of the configuration commands inside the unit – the 8x SpaceWire codecs – the AFE control logic required to configure it when unit is switched on – the clock / sync logic required to manage both external (nominal) and internal (back-up) clock and sync signals.

All the above functions are implemented in a OTP radiation tolerant FPGA.

Note: dialog between integrated AFE and digital electronics is relying on LVDS electrical interface without the use of external CMOS to LVDS translator. SpaceWire interface is relying also on LVDS but since it is an external interface external LVDS translators are implemented.

- Housekeeping electronics: encompasses currents sources to bias the temperature probe – amplifiers to adapt housekeeping range to A to D converter range – multichannel A to D converters.
• Power conditioning electronics: encompasses low dropout voltage linear regulators required to limit the effect of very long external harnesses on the functions and performance of the unit – EMC filters to limit effect of noise pick-up along the external harnesses on the performance of the unit.

5.3.2.4.2 Mechanical Layout

The mechanical layout of the unit shall be defined in order to avoid any degradation of the performances. In particularly, high capacitance phase drivers generate high currents, which may propagate in the low noise analog processing electronics. Such high currents shall be not only decoupled but also mechanical layout shall not lead to excessive signal routing length. Identical layout for the 4 detector electronics is also desirable to avoid performance dispersion.

The next figures depict the F-FEE layouts. Two options are currently evaluated. In option 1 the top board is hosting the 4 analog electronic block (1 per detector) including analog processing channels and clock / bias electronics. Then in the middle a second board hosts the digital electronics (mainly a FPGA). Finally the bottom board hosts the housekeeping and power supply electronics. In option 2 the two top boards are hosting the 4 analog electronic blocks (two per board) while the bottom board hosts the digital / housekeeping and power supply electronics. Options have not impact on unit dimensions.

5.3.2.5 EXTERNAL INTERFACES

5.3.2.5.1 Electrical Interfaces

The following table summarizes the electrical interface of the unit, including main characteristics.

<table>
<thead>
<tr>
<th>Interface type</th>
<th>With</th>
<th>Interface characteristics</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Command / data</td>
<td>FEU</td>
<td>SpaceWire: 100 Mbps downstream – tbd upstream</td>
<td>8</td>
</tr>
<tr>
<td>Clock / Sync</td>
<td>F-AEU</td>
<td>Clock: LVDS – 50 MHz Sync: LVDS – 2.5 s</td>
<td>1</td>
</tr>
<tr>
<td>Power interface</td>
<td>F-AEU</td>
<td>6x secondary power lines</td>
<td>1</td>
</tr>
<tr>
<td>Detector</td>
<td>F-FPA</td>
<td>Bias / 40-MHz clocks / 4-MHz analog output</td>
<td>4</td>
</tr>
</tbody>
</table>
### Power budget (W)

<table>
<thead>
<tr>
<th>Mode</th>
<th>Mean</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stand-by</td>
<td>10.36</td>
</tr>
<tr>
<td>Frame transfer</td>
<td>24.76</td>
</tr>
<tr>
<td>Register readout</td>
<td>12.16</td>
</tr>
</tbody>
</table>

### Mechanical Interfaces

The unit has mechanical interface with the OB only. The following table sums-up the mechanical property of the unit:

<table>
<thead>
<tr>
<th>Dimension</th>
<th>185 mm (Xcam) x 193 mm (Ycam) * 75 mm (Zcam)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mass</td>
<td>1.400 kg, w/o margin</td>
</tr>
<tr>
<td>Mounting</td>
<td>4x M4 bolts (TBC)</td>
</tr>
</tbody>
</table>

### Thermal Interface

The unit has conductive thermal interface with the OB (or camera support) and radiative thermal interface with its environment. The following table sums-up the thermal property of the unit:

<table>
<thead>
<tr>
<th>Conduction surface</th>
<th>Base plate: 35700 mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiative surface</td>
<td>Flanges + top cover: 66885 mm²</td>
</tr>
<tr>
<td>Emissivity</td>
<td>&gt; 0.85</td>
</tr>
</tbody>
</table>

### PROTOTYPING

A prototype is currently in preparation. It aims in the validation of critical items. Therefore the prototype will focus on:

- 1-the data / command interface with the FEE
- 2-the detector clock sequencer
3-the phase drivers

The next figure depicts the prototype block diagram based on the assembly of ‘modules’ (an FPGA board for items 1 and 2 – a specifically designed board for items 3 – a prototype board for analog processing electronics).

### 5.3.2.7 EEE MAIN PART LIST

Main EEE active parts are listed in the next table. Reference, provider, package and radiation tolerance are indicated. No critical item is identified except the fact that some of the references are available only from a single source. However alternative designs exist (i.e. non-integrated AFE) and obsolescence of parts would increase design effort rather than becoming a showstopper for the design of the unit.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
<th>Provider</th>
<th>Package</th>
<th>Radiation</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD8138</td>
<td>Fast analog diff receiver</td>
<td>AD</td>
<td>10-pin FP</td>
<td>100 krad</td>
</tr>
<tr>
<td>LM98640QML</td>
<td>Dual integrated 14-bit AFE</td>
<td>NS</td>
<td>68-pin CQFP</td>
<td>100 krad</td>
</tr>
<tr>
<td>ISL7457SRH</td>
<td>Quad clock driver</td>
<td>Intersil</td>
<td>16-pin FP</td>
<td>10 krad</td>
</tr>
<tr>
<td>DAC121S01QML</td>
<td>12-bit D to A converter</td>
<td>NS</td>
<td>10-pin FP</td>
<td>100 krad</td>
</tr>
<tr>
<td>LM484S</td>
<td>High voltage AOP</td>
<td>AD</td>
<td>14-pin FP</td>
<td>100 krad</td>
</tr>
<tr>
<td>ADC128S102QML</td>
<td>8-channel 12-bit A to D</td>
<td>NS</td>
<td>16-pin FP</td>
<td>100 krad</td>
</tr>
<tr>
<td>RTAX1000SL</td>
<td>Rad tol OTP FPGA</td>
<td>ACTEL</td>
<td>352-pin CQFP</td>
<td>300 krad</td>
</tr>
<tr>
<td>SNV55LVDS31/32W</td>
<td>LVDS</td>
<td>TI</td>
<td>16-pin FP</td>
<td>75 krad</td>
</tr>
<tr>
<td>RHF4913A</td>
<td>Linear voltage regulator</td>
<td>STm</td>
<td>16-pin FP</td>
<td>300 krad</td>
</tr>
<tr>
<td>AD590</td>
<td>Temperature probe</td>
<td>AD</td>
<td>2-pin FP</td>
<td></td>
</tr>
</tbody>
</table>

### 5.3.3 AEU (N AND F)

#### 5.3.3.1 AEU OVERVIEW AND INTERFACES

The N-AEU and F-AEU boxes are located in the SVM. The distance between them and the FEE boxes is up to 5 meters.

There are 4 N-AEU boxes, one for each camera group. Each box contains 8 independent DC/DC converters; each converter is dedicated to one N-FEE.

There is 1 F-AEU box for the 2 F-FEES. It contains 2 fully independent DC/DC converters, one for each F-FEE.

The N-AEU (or F-AEU) system shall provide to each N-FEE (or F-FEE) the following main signals:
- 6 DC voltages, supplied by a dedicated DC/DC converter,
- a set of synchronisation signals, used by the N-FEE (or F-FEE) for the CCD activity management.

To do this, each N-AEU system receives from the SVM:
- 2 regulated power lines at 28V
  - one for the DC-DC converter part, dedicated to power the N-FEEs,
  - one low power used for the system logic part,
- 2 (i.e. one Main and one Redundant) master clock signal links at 50 MHz,
- 2 (i.e. one Main and one Redundant) synchronisation signal links at 1.25 s.

More, each N-AEU system receives from the ICU:
- 2 SpaceWire links, one main and one redundant links,
- 2 (i.e. one Main and one Redundant) discrete command lines.

The F-AEU system, on its side, receives from the SVM:
- 2 regulated power lines at 28V,
- 2 (i.e. one Main and one Redundant) master clock signal links at 50 MHz,
- 2 (i.e. one Main and one Redundant) synchronisation signal links at 1.25 s,

The F-AEU system receives from the ICU, 4 SpaceWire, two main and two redundant links.
AEU interfaces
5.3.3.2 AEU REQUIREMENTS

5.3.3.2.1 Secondary voltage requirements

The table shows the worst case, where all circuits are powered continuously (see FEE section for an alternative possibility) in order to achieve the required performance:

<table>
<thead>
<tr>
<th></th>
<th>VCCD</th>
<th>VCLK</th>
<th>VAN1</th>
<th>VAN2</th>
<th>VAN3_NEG</th>
<th>VDIG_FPGA</th>
<th>VDIG_SpW</th>
<th>Ptot</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>BOL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak currents mA</td>
<td>86.3</td>
<td>158.2</td>
<td>168.3</td>
<td>147.7</td>
<td>147.4</td>
<td>855.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mean power mW in N-FEE and cables</td>
<td>2206.3</td>
<td>890.8</td>
<td>828.3</td>
<td>433.6</td>
<td>725.4</td>
<td>1831.8</td>
<td>6916.4</td>
<td></td>
</tr>
<tr>
<td><strong>EOL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Peak currents mA</td>
<td>95.0</td>
<td>174.0</td>
<td>185.2</td>
<td>162.4</td>
<td>162.2</td>
<td>941.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mean power mW in N-FEE and cables</td>
<td>2427.0</td>
<td>979.9</td>
<td>911.2</td>
<td>477.0</td>
<td>797.9</td>
<td>2015.0</td>
<td>7608.0</td>
<td></td>
</tr>
</tbody>
</table>

5.3.3.2.2 DC/DC synchronization requirements

It shall be possible to synchronise the DC-DC converters with a clock signal at 125 kHz (TBC), issued from the master 50 MHz reference clock.

5.3.3.2.3 Differential noise and ripple requirements

<table>
<thead>
<tr>
<th>DM noise &amp; ripple (pk-pk), 10 Hz to 50 MHz</th>
<th>VCCD</th>
<th>VCLK</th>
<th>VAN1</th>
<th>VAN2</th>
<th>VAN3</th>
<th>VDIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 mV</td>
<td>10 mV</td>
<td>10 mV</td>
<td>10 mV</td>
<td>10 mV</td>
<td>10 mV</td>
<td>10 mV</td>
</tr>
</tbody>
</table>

Common mode (CM) filters, noise and ripple requirements:

- CM noise and ripple shall be reduced by means of a suitable CM filter on each output, within the AEU.
- Each CM filter shall be located as close as possible to the transformer, to minimize the loop area of CM switching noise current spikes.

<table>
<thead>
<tr>
<th>CM noise &amp; ripple (rms), 10 Hz to 50 MHz, measured with an AC load resistance of 0.1 ohm</th>
<th>VCCD</th>
<th>VCLK</th>
<th>VAN1</th>
<th>VAN2</th>
<th>VAN3</th>
<th>VDIG</th>
</tr>
</thead>
<tbody>
<tr>
<td>21 uV</td>
<td>21 uV</td>
<td>21 uV</td>
<td>21 uV</td>
<td>21 uV</td>
<td>21 uV</td>
<td>21 uV</td>
</tr>
<tr>
<td>A total of 125 uV rms</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>125 uV rms can be shared equally as 21 uV rms per output, or in some other combination, which is far more likely.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.3.3.2.4 Line regulation requirements

A step of the primary voltage from 27 V to 29 V shall produce a change lower than 0.1% on the output voltage.

There shall be no significant overshoot or undershoot, i.e. <5% of the nominal voltage on each output. Measurements shall be made on 50% load and full load.

5.3.3.2.5 Crosstalk requirements

The maximum crosstalk from any one output (culprit) to any other output (victim), for a load step from 50% to 100% with <1 µs rise time on the culprit output, shall be lower than:

- for analogue voltage outputs (VCDD, VCLK, VAN1, VAN2): 1% (TBC)
- for the digital voltage output (VDIG): 2% (TBC)

5.3.3.2.6 Isolation, shielding, grounding requirements

There shall be galvanic isolation between the primary and all secondary windings of the transformers.

All secondary outputs windings shall be isolated from each other, with no direct connection to the structure ground.

The primary winding of the isolation transformer shall be shielded from the secondary windings by a conductive electrostatic shield, which can be connected to a local ground star point, which in turn is connected to the structure.

It shall be assumed that each harness connected to a power input or output connector will have an outer shield connected to the structure via the connector body/backshell. In order to prevent problems associated to radiated EMI from small loops of bonding wires inside the units, there will be no pins designated as outer shield connections within the AEU connectors.

There shall be no direct connection of any secondary output to the ground star point or structure.

Grounding to structure of the secondary outputs is performed within the N-FEE (or F-FEE), at the connection to the CCDs.

5.3.3.2.7 Synchronization signals requirements

For the N-FEE, the N-AEU shall provide:

- a low frequency signal with a temporal period of: 6.25 s, and with one top on 4 longer to indicate the beginning of the 25 s cycle,
- a 50 MHz clock frequency.

For the F-FEE, the F-AEU shall provide:
- a low frequency signal with a temporal period of 2.5 s (this signal being synchronised on the 25 s activity of the N-FEE)
- a 50 MHz clock frequency.

Next figure indicates the synchronization data between the signals.

**Synchronization signals description**

### 5.3.3.3 AEU ARCHITECTURE

The following figure shows the N-AEU architecture resulting from the study, compliant with all requirements.
In result, the N-AEU design is based on a development of two types of modules, the N-FPGA module and the DC-DC converter module. In total, the N-AEU consists in an assembly of 2 N-FPGA modules including one in cold redundancy and 8 DC-DC converter modules (one for each N-FEE).

The functionalities of the N-FPGA module are:

- the SpaceWire interfaces control,
- the 6.25 s and 25 s synchronisation pulses generation from 1.25 s and 50 MHz signals,
- the ON/OFF, limitation and protections of the DC-DC converters
- the status and commands management,
- the generation of the synchronisation frequency of the converters,
- the housekeeping internal interface, digital conversion and transmission of the HK to ICU over the SpaceWire network.

A trade-off is still in progress on the N-FPGA Module command. The 2-power line architecture presented here requires discrete relay commands that can come from the ICU. Another possibility would be to request a third (low) power line from the SWM; in this case, each N-FPGA module would be supplied by its own power line.

The block diagram is described the next figure.
The functionalities of the converter module are:

- the DC voltage generation of the 6 outputs across Half-Bridge converter cell,
- the input protection of the DC-DC converter,
- input and output filters,
- linear post regulation,
- the inner housekeeping generation and interface with the FPGA module.

The block diagram of this module is described in the following figure.
Converter module block diagram

For the F-AEU, the architecture is based on two independent chains for power supply. It consists in the assembly of 2 F-FPGA Modules and 2 Converter Modules.

The functionalities of the F-FPGA Module are:

- the SpaceWire interfaces control,
- the 2.5 s synchronisation signal generation from 1.25 s and 50 MHz signals,
- the generation of the synchronisation frequency of the DC-DC converters
• the housekeeping internal interface, digital conversion and transmission of the HK to ICU over the SpaceWire network.

The converter Module has the same functions as in the N-AEU

5.3.3.4 AEU MECHANICS

Each module (Converter and FPGA) is fixed by screws on a specific 2-mm thick aluminium structure (mechanical structure only on the edges).

The FPGA Module has an armour-plate screwed on the mechanical structure. There are 3 inputs connectors (SUBHD) and 2 outputs connectors (SUBHD) on the FPGA modules.

The Converter Module will not have this armour-plate, and will have only one output connector (SUBHD).

Each mechanical structure may have brackets (TBD according to the thermal analysis).

The mechanical structure will be connected together by “pins mortises” to break the leakage lines and fixed by screws. A stainless steel rod will connect all modules at each corner (TBD according to the thermal analysis).

Converter module overview

The external mechanical structure will have a shutting plate of 2mm thick.

The output connectors (SUBHD) will be welded on the PCB in the most of cases and fixed on the mechanical structure.
Interconnection between the modules will be done by connectors (TBD) welded on one hand on the FPGA and converter module and on the other hand on the Flex map. All will be closed by an aluminium lid screwed and fitted by “pins mortises”.

5.3.3.5 N-AEU AND F-AEU DIMENSIONS

The N-AEU box has presently the following dimensions, which are TBC:
- For the base plate: 315 mm x 185 mm
- For the height: 185 mm

These dimensions are without protrusions and connectors.

The F-AEU box has presently the following dimensions, which are TBC:
- For the base plate: 315 mm x 85 mm
- For the height: 185 mm

These dimensions take into account protrusions and connectors.

5.3.3.6 N-AEU AND F-AEU DIMENSIONS

The N-AEU and F-AEU powers given in [AD3] are based on a hypothesis of ~40 % (including some design maturity margin) conversion loss (~3 % for the N-AEU, +3 % for the F-AEU which sees higher peak power), and 7 W for the low level electronics.

5.4 ON BOARD DATA TREATMENT

5.4.1 MEU AND N-DPU

This section gives an overview of the MEU and N-DPU design.

5.4.1.1 MEU OVERVIEW

A MEU gathers in the same box:

- 4 N-DPU boards: each N-DPU board is responsible for handling two normal cameras.
- 2 SpaceWire routers: one main and one redundant.
- A Power Supply Unit that convert the primary voltage received from the SVM into the secondary voltages needed for powering the N-DPU boards and the routers.
- A Motherboard

The figure below describes the preliminary architecture of a MEU box:
Each N-DPU board is connected to 2 N-FEE thanks to 4 SpaceWire links configured to run at 100 Mbps (one SpaceWire link per CCD readout output).

Each N-DPU board is connected to the nominal router and to the redundant router.

Nominally, both MEU routers are working in cold redundancy. But, to handle certain failure cases, both MEU routers can be switched on simultaneously and can work in hot redundancy.

Two SpaceWire test interface ports will be available: the first is connected to the Router-M and the second to the Router-R.
5.4.1.2 MEU INTERFACES AND DATA RATES

5.4.1.2.1 N-DPU / N-FEE interface

5.4.1.2.1.1 Synchro signal between N-FEE and N-DPU

5.4.1.2.1.1.1 6.25-sec synchro

The 6.25-sec synchro top received by the N-FEE (which is used by the N-FEE to start the CCD readout) is forwarded to the N-DPU by the N-FEE as a SpaceWire time-code. The time-code is produced by the N-FEE TBD µs after the reception of the 6.25-sec synchro top.

When the N-DPU receives the « 6.25-sec synchro top time-code », it makes a snapshot of its current internal time: the N-DPU will use this time snapshot:

- to time-stamp the data produced from the CCD image (star flux and centroids, raw imagettes).
- to time-stamp the HK and status sent by the N-FEE

The N-DPU has to choose on which SpaceWire link the time-code is emitted thanks to a configuration command sent to the N-FEE (link1, link2, no_link).

The N-DPU will start the processing of the CCD images 3 seconds after the reception of the 6.25-sec synchro top (processing triggered by a software timer).

5.4.1.2.1.1.2 25-sec synchro

Within the current design, the N-DPU doesn’t need to know the 25-sec synchro. However, for future needs, this information will be transmitted by the N-FEE implementing the following mechanism:

- the N-FEE starts the transmission of the time-code upon the 25-sec synchro
- if the time_code_value modulo 4 = 0, then the 6.25-sec synchro top corresponds to a 25-sec synchro.

5.4.1.2.1.2 Pixel data transmission from N-FEE to N-DPU

The N-FEE transfers the pixel data to the N-DPU thanks to RMAP write commands (Write non-acknowledged, non-verified mode).

At the N-DPU side, the RMAP protocol will be fully handled by a dedicated hardware module (no software intervention).

Each CCD half line (2255 pixels + 25 prescan pixels) will be transferred by the N-FEE to the N-DPU memory as one RMAP write command.
The pixels will be coded on 16 bits. At the N-FEE level, the pixels will be digitized with 14-bit ADC but the N-FEE will add 2 padding bits to these 14 bits before transmitting the pixels to the N-DPU so that the values received by the N-DPU are aligned on 16 bits.

Before each transferred half line, a 16-bit word containing a 6.25-sec top counter will be added. By reading this counter, the N-DPU software will be able to know if the data corresponds really to a line of the current 6.25-sec cycle or to a line of the previous 6.25-sec cycle. This allows detecting a problem of transmission (missing data). The 2 MSB of the counter could be used to tag the ID of the CCD (0, 1, 2 or 3).

5.4.1.2.1.3 Transmission of the HK and N-FEE status to N-DPU

Two modes of transmission will be implemented:
- On request:
  o RMAP read command from N-DPU to N-FEE
  o Sporadic command useful for test and configuration operations
- Automatic:
  o No request from the N-DPU
  o Nominal mode (scientific mode)
  o On the reception of the 6.25-sec synchro top, the N-FEE will make a snapshot of the HK and status.
  o This snapshot (a block containing all the HK and status) will be transmitted just after the last pixel (appended to the image).
  o RMAP write command from the N-FEE to the N-DPU (Write non-acknowledged, non-verified mode)

5.4.1.2.1.4 Command transmission

The commands sent by the N-DPU to the N-FEE will be implemented as RMAP write commands from the N-DPU to the N-FEE (write acknowledged / verified mode).

5.4.1.2.1.5 Data rates

The instantaneous data rate between 2 x N-FEE and N-DPU is: $2 \times 2 \times 4 \text{ Mpx/s} \times 1.25 = 4 \times 80 = 320 \text{ Mbps}$.

With two SpaceWire links between 1 N-FEE and 1 N-DPU, the instantaneous data rate over one link is: $80 \text{ Mbps}$. This throughput (80 Mbps) is compatible with a SpaceWire link configured to run at a bit rate of 100 Mbps.

The channel utilization is 80%. Taking into account that the transmission can be smoothed during the CCD line transfer time (80 µs per line), the data rate averaged over 2.94 seconds (i.e. over the full-frame image readout time) is 70 Mbps per link and the channel utilization is 70%.
5.4.1.2.2 MEU / ICU interface

5.4.1.2.2.1 Data rates

The data rates given below include: a 50% margin on star count, the SpaceWire overhead and the packetization overhead.

The data rate between one N-DPU and the MEU router is: 735 kbps. That corresponds to the transmission of about 21 packets per second.

The data rate between one MEU and the active ICU is: 4 x 735 kbps = 2.9 Mbps. That corresponds to the transmission of about 83 packets per second.

5.4.1.3 N-DPU SOFTWARE DESIGN

5.4.1.3.1 Overview

The N-DPU flight Software will be made up of two different and complementary products: the Boot Software and the Application Software.

5.4.1.3.1.1 Boot software

The Boot Software is the critical and low complex software which will be responsible for the boot of the Application Software. The Boot Software will be stored in the N-DPU PROM.

After a switch-on or a reset (software or hardware), the N-DPU goes to a “safe” mode. In this mode, the flight software which will be activated is the Boot Software. The Boot Software communicates with the ICU through a SpaceWire link.

The N-DPU Boot Software shall load the Application Software code and data from the SpaceWire link. After a switch-on or a N-DPU reset (software or hardware), the Boot Software is waiting for S/W code and data packets from the ICU.

The ICU shall be responsible for:

- managing the maintenance of the N-DPU application S/W,
- managing the content of the EEPROM,
- sending to the N-DPU, over the SpaceWire link, the application S/W code and data packets which will be loaded by the DPU boot loader during the boot process.

The N-DPU Boot Software shall be responsible for:

- handling the load of the data / code from the SpaceWire link,
- checking the integrity of the data / code loaded by mean of checksums,
- starting the application Software.
5.4.1.3.1.2 Application software

The Application Software corresponds to the scientific software. It implements all the technical and scientific functionalities which are required by the mission. It will be stored in the ICU EEPROM. It will be loaded in the N-DPU SRAM through the SpaceWire network and started upon a ground telecommand thanks to the N-DPU Boot Software.

The N-DPU Application Software will be fully reconfigurable at the ICU EEPROM level thanks to the TC-driven memory upload functionality of the ICU Software.

5.4.1.3.2 Common services

The N-DPU Application Software shall implement the following common services:

- Handle the communication with the ICU.
- Handle the interface with the N-FEE (data, commands, HK).
- Produce scientific data (PLTM) according to the active mode: Flux, Centroids, Imagettes (imagettes are rectangular window containing the image of one star), and full-frame images.
- Manage a set of star descriptors built from a star catalogue handled at the ICU level.
- Produce state and diagnosis information which is transmitted in HKTM packets: SW status, N-DPU HW status, Command acknowledgments, Memory dumps, Event reports, Failure reports…
- Manage the software parameters. The individual software parameters or constants can be individually changed by dedicated command from Ground. An image of the software parameters can be dump in HKTM.
- Receive the onboard time from the ICU and handle the time stamping of HKTM and scientific data.
- Execute the mode changes decided by the ICU: the mode changes are triggered upon the reception of a command from ICU.
- Handle a software reset: The triggering of the software reset causes the stop of Application Software and the starting of Boot Software.
- Manage the watchdog.
- Help to the maintenance of the N-DPU application software thanks to memory check / memory dump / memory upload services.

5.4.1.3.3 Observation mode processing

In the observation mode, the processing is done in fours steps:

<table>
<thead>
<tr>
<th>Processing</th>
<th>Cadence</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Full-frame image acquisition (x2)</td>
<td>6.25 sec.</td>
<td>Hardware</td>
</tr>
<tr>
<td>2. Window extraction</td>
<td>6.25 sec.</td>
<td>Software</td>
</tr>
<tr>
<td>3. Data correction and reduction</td>
<td>6.25 sec.</td>
<td>Software</td>
</tr>
<tr>
<td>4. Updating of photometric masks and star positions</td>
<td>5400 sec.</td>
<td>Software</td>
</tr>
</tbody>
</table>
5.4.1.3.3.1 Full-frame image acquisition

The data volume transferred from N-FEE to each N-DPU is 2.64 Gb (165 Mb x 2 x 4) over a period of 25 sec.: that corresponds to the transfer of 2x4 full-frame CCD.

For the normal cameras, the size of one full-frame CCD image including n=50 prescan columns (n is TBC) and m=10 overscan rows (m is TBC) is: \((4510 + n) \times (4510 + m) \times 16\) bits = 330 Mb.

The 4 full-frame CCD images of each camera are transferred sequentially and not simultaneously according the following cycle:

![Normal camera CCD image transfer cycle and N-DPU computing tasks](image)

In the 25-sec. cycle, two full-frame CCD images (330 Mb) will be transferred every 6.25 sec from the both N-FEE to the N-DPU over four SpaceWire links at a data rate of \(4 \times 4\) Mpx/s x 1.25 = 320 Mbps, i.e. 80 Mbps per link (the 25 % margin covers the SpaceWire overhead and the RMAP headers).

Each CCD full-frame image is stored in the N-DPU SDRAM memory before processing. The transfer and storage operation will be done transparently from the software point of view thanks to DMA/RMAP technology. Since the 4 full-frame CCD images of each camera are transferred sequentially, the N-DPU memory can be sized to work with only one full-frame image at a time during the observation mode.
5.4.1.3.3.2 Window extraction

The window extraction process consists in defining a window around each star in the full-frame image zone and to copy the content of this window to a different memory location where the processing will be performed. See below an example of a 94x94-pixel CCD zone with the star windows and an example of the content of a 6x6-pixel star window:

![Windowing example](image1)

![Content of a 6x6-pixel star window](image2)

The window extraction process is triggered as soon as a CCD full-frame image is available in the N-DPU memory: it is triggered four times over a period of 25 seconds. This extraction is performed using a set of windows descriptors (position, size of the window, star magnitude, etc.) computed in configuration mode.

The extracted windows can be rectangular or can match exactly the photometric masks (useful pixels). The basic window size is: 36 pixels (6x6 pixels).

The count of the extracted windows is the following (the count is given for the 4 CCDs of the both cameras:

<table>
<thead>
<tr>
<th>Sample P1</th>
<th>2x6720, with margin 50% = 2x10080</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample P4</td>
<td>2x102200, with margin 50% = 2x153300</td>
</tr>
<tr>
<td>Background windows</td>
<td>2x400</td>
</tr>
<tr>
<td>Imagettes</td>
<td>up to 2x2000</td>
</tr>
<tr>
<td>Offset windows</td>
<td>2 x 2 x 4 offset windows (2255 pixels)</td>
</tr>
<tr>
<td>Smearing rows</td>
<td>2 x 4 x 10 overscan rows</td>
</tr>
</tbody>
</table>

The distribution of the stars among the 4 CCDs is not homogenous. A factor 2 is possible between the most populated CCD and the least one.
5.4.1.3.3.3 Data correction and reduction

The data reduction process is triggered as soon as a set of windows extracted from a full-frame image is available. It is made up of the following steps:

- Compute two offset values per half CCD. The bad pixels of the raw offset windows are detected using a statistical criterion based on the computation of the median and the variance.
- Subtract the offset value from the smearing rows, the star windows and the background windows.
- Compute an array of smearing values. One value of smearing is computed per CCD column (4510 values). Before computing the smearing values, the bad pixels are detected and removed.
- Subtract the smearing from the star windows and the background windows using the smearing value array.
- Subtract the background from the star windows using a background model computed in the Configuration mode.
- Compute the background values (~400 values). These values are not used to subtract the background in real-time but to monitor the background evolution and to update the background model.
- Compute the flux for each star window: the photometric algorithms will be based on the weighted mask method which gives the best results for the normal camera configuration. The photometric masks are computed in the configuration mode and periodically updated in the observation mode (see section below).
- Correct the flux values from the gain of the detector (2 gain values per CCD). All the corrected flux values (up to 2 x 163380 x 24 bits / 25 sec) are sent to the ICU.
- Compute the star centroid for each star window belonging to the Sample P1 and for a fraction (1 %) of the stars belonging to P4. All the centroid values (up to 2 x 11610 x 2 x 16 bits / 25 sec) are sent to the ICU. The computation of the centroids is performed with the COB method (Center Of Brightness).
- Transmit to ICU the imagette windows (up to 2 x 2000 imagette windows). The size of an imagette window is 6x6-pixels.

The outlier detection is done at the normal N-DPU level just for the offset, smearing and background windows. Concerning the light curves and the centroid curves, the outlier detection will be done at the ICU level.

Since all the curves are downloaded individually, it is not necessary to perform the jitter correction on-board: the jitter correction will be handled at the ground segment level.

5.4.1.3.3.4 Updating of photometric masks and star positions

Three operations shall be done periodically for each star:

- Updating the mask position. The objective is to anticipate the star displacement by computing the position the star will have at the middle of the time interval between two successive updates.
• Updating the mask itself by using a gaussian analytic model of the PSF.
• Updating the normalisation of the mask.

The frequency of the updating operation depends on the position of the star in the FoV. The worst case corresponds to the stars located at the edge of the FoV. In this case, the weighted masks shall be updated every 1.5 hours (5400 sec.).

5.4.1.3.4 Configuration mode processing

In the configuration mode, the operations are split in the following steps:

1) Acquire "Far field" full images (summation of n CCD full images which have been previously corrected from offset and smearing).
2) Identify the list and the raw positions of the reference stars (brightest stars but not saturated).
3) Compute a background model (search for local minimums and computation of a background model by performing a 2D polynomial fit).
4) Compute the accurate positions of the reference stars and the distortion matrix
5) Compute for each reference star the parameters of the PSF model.
6) Identify all the targets and derive their accurate positions.
7) Derive the parameters of the PSF associated with all the targets.
6) Compute the masks and the window positions of all targets.

5.4.1.3.5 Power processing estimation

5.4.1.3.5.1 Assumptions

The processing power has been estimated by prototyping the main algorithms in C language on a LEON2@100 MHz processor simulator.

The estimation of the required computation power has been done taking into account the following assumptions:

- The transfer and the storage of the full-frame images in the N-DPU memory are done without involving the N-DPU processor, that is to say without involving the software (the CPU occupation rate needed to acquire the full-frame images is negligible). This assumption implies that the N-DPU hardware module in charge of the image transfer relies on a RMAP / DMA hardware controller.
- The CPU budget has been estimated by using the weighted mask photometry and the COB algorithm for the centroid computation.
- The following optimizations have been implemented:
  o The main algorithms are computed using 32-bit integers instead of floating point values.
  o The photometric algorithms are applied on non-rectangular windows (in order to reduce the number of pixels to process).
- The number of targets processed is compliant to the scientific requirements in terms of star count with the 50% margin.
- The frequency of the mask updating has been set to 5000 sec.
- One wait-state has been programmed on the RAM access (write and read).

5.4.1.3.5.2 Conclusion

The CPU occupation rate which has been measured is 37% (CPU load margin = 170%). This occupation rate is compatible with a margin on the CPU load better than 100 % at the PDR. The conclusion is that the normal N-DPU board can be implemented with one LEON processor working at 100 MHz.

The existing CPU load margin could be used to improve the algorithms, to implement new algorithms, to process more targets, to update with a higher frequency the photometric masks or to reduce the processor frequency (with a LEON at 80 MHz, the CPU load is 46% and the CPU load margin is 116%).

5.4.1.3.6 Memory budget

The table below summarizes the need in terms of memory resources.
Program + Data (SRAM)

4 MBytes

<table>
<thead>
<tr>
<th>Mass storage (SDRAM)</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>2 full-frame images (4510+50)x(4510+10)x(16 bits)</td>
<td>660 Mb</td>
<td>82.4 MBytes</td>
</tr>
<tr>
<td>The memory is sized to be able to store one full-frame image per camera at a time.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 x N 6x6-mask (32 bits)</td>
<td>251 Mb</td>
<td>31.4 MBytes</td>
</tr>
<tr>
<td>Photometric masks (one per star)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 x N window and star descriptors (36x32-bit parameters)</td>
<td>251 Mb</td>
<td>31.4 MBytes</td>
</tr>
<tr>
<td>One per star or technical window. Each descriptor is made up of 36 parameters. The star descriptors contain data from the star catalogues and data computed on-board.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 x N 6x6-windows (32 bits)</td>
<td>251 Mb</td>
<td>31.4 MBytes</td>
</tr>
<tr>
<td>Temporary working buffers (buffer where the star windows are copied from the fullimage zone).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 x N pre-computed background values (float)</td>
<td>7.0 Mb</td>
<td>0.9 MBytes</td>
</tr>
<tr>
<td>The output buffer are sized to store 25 seconds of acquisition 1.5 * (25 * output rate kbps).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output packet buffers</td>
<td>14.7 Mb</td>
<td>1.8 MBytes</td>
</tr>
<tr>
<td>20 mask computation coefficients for 2 x N stars (float)</td>
<td>139.4 Mb</td>
<td>17.4 MBytes</td>
</tr>
<tr>
<td>Coefficients used to compute the photometric masks.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total / N-DPU</td>
<td>1574 Mb</td>
<td>196.7 MBytes</td>
</tr>
<tr>
<td>with 50 % margin on star count</td>
<td>2030 Mb</td>
<td>253.8 MBytes</td>
</tr>
</tbody>
</table>

Assumptions

| Floating-point coding (single precision = 32 bits double precision = 64 bits)       | 32    |
| Number of stars N per camera (without margins)                                     | 108920 |
| Number of camera per DPU                                                           | 2     |
| Full image number per camera                                                       | 1     |
| DPU->ICU data rate (kbps)                                                          | 588   |

5.4.1.4 MEU HARDWARE DESIGN

In the following paragraphs the HW architecture of the MEU boards is described.

5.4.1.4.1 Motherboard

The Motherboard has two main objectives:

- Performs the internal connections between all the boards of the MEU box.
- Also provides physical support to the other boards.
5.4.1.4.1.1 HW Implementation

The Motherboard includes only MHD 100 female (TBC) connectors where the rest of the boards are plugged in. This PBA connects the internal signals of the MEU equipment that have to be passed between boards. Next figure shows the connectors located in the Motherboard.

![MotherBoard Layout]

5.4.1.4.1.2 External Connectors

The Mother board has not external interfaces. All the external connectors are located in the other boards.

5.4.1.4.1.3 Internal Connectors

The Mother board has the following internal connectors:

<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MHD 100S</td>
<td>Interface with N-DPU1</td>
<td>Motherboard</td>
<td>N-DPU1</td>
</tr>
<tr>
<td>MHD 100S</td>
<td>Interface with N-DPU2</td>
<td>Motherboard</td>
<td>N-DPU2</td>
</tr>
<tr>
<td>MHD 100S</td>
<td>Interface with N-DPU3</td>
<td>Motherboard</td>
<td>N-DPU3</td>
</tr>
<tr>
<td>MHD 100S</td>
<td>Interface with N-DPU4</td>
<td>Motherboard</td>
<td>N-DPU4</td>
</tr>
<tr>
<td>MHD 100S</td>
<td>Interface with SpW Router_M</td>
<td>Motherboard</td>
<td>SpW Router_M</td>
</tr>
<tr>
<td>MHD 100S</td>
<td>Interface with SpW Router_R</td>
<td>Motherboard</td>
<td>SpW Router_R</td>
</tr>
<tr>
<td>MHD 100S</td>
<td>Interface with PSU</td>
<td>Motherboard</td>
<td>PSU</td>
</tr>
</tbody>
</table>
5.4.1.4.1.4 Mechanical layout and budgets

The size of this board will be 130 x 233,35 mm.

5.4.1.4.2 SpaceWire Router Board

The SpW Router board is in charge of routing the information between the ICUs (M and R) and all the elements of the MEU. Two Routers have to be included in the MEU, Main and Redundant, in order of increasing the reliability of the system.

The data to be changed between the MEUs and the ICUS are:

- The SpaceWire routers configuration commands
- The N-DPUs configuration commands
- The switch on/off commands for the PSU
- The HK and status TM from the N-DPUs
- The HK and status TM from the N-FEEs (sent by the corresponding N-DPU).
- The HK and status TM from the PSU
- The HK and status TM from the SpW Routers
- The scientific data from the N-DPU

To allow all these information exchanges the SpW Routers (both M and R) has to be connected with the four N-DPUs, the PSU and the corresponding ICU (the main Spw Router is connected with the main ICU and the redundant router with the redundant ICU).

Also both routers are connected each other (not in the normal operation but in special circumstances) and they include besides an external Test connector. Therefore each Router contains eight SpW ports. In the block diagram of paragraph 5.4.1.1 the two SpW Routers are drawn, detailing the links between them and the other elements in the MEU and ICU equipments.

5.4.1.4.2.1 HW Implementation

The main hardware elements of the SpW Router board are:

- SpW links (connectors and transceivers): compliant with the standard ECSS-E-ST-50-12C.
- SpW-10X ASIC (AT7910F): This ASIC performs the main functions of the router.
SpaceWire Router HW Architecture

The SpaceWire connector has eight signal contacts plus a screen termination contact. A nine-pin female micro-miniature D-type is specified as the SpaceWire connector. This type of connector is available qualified for space use.

5.4.1.4.2.1 ASIC AT7910F

The AT7910E provides a routing capability between eight SpaceWire links according to the SpaceWire Standard ECSS-E-50-12A.

The eight SpW ports allow the communication between the next modules:

- ICU
- N-DPU1
- N-DPU2
- N-DPU3
- N.DPU4
- PSU
- Test Port
- The other SpW Router (main and redundant routers connexion)
The AT7910E is manufactured using the SEU hardened cell library from Atmel MH1RT CMOS 0.35µm radiation hardened sea of gates technology.

The SpaceWire router comprises the logic blocks that are shown in the figure included in paragraph 5.4.1.4.2.1. From all the blocks of the ASIC those that are going to be used in the MEU SpW Router board are:

- Eight SpaceWire bi-directional serial ports.
- A non-blocking crossbar switch connecting any input port to any output port.
- An internal configuration port accessible via the crossbar switch from the SpaceWire input/output ports. The Remote Memory Access Protocol (RMAP) is used to access the configuration port. The Router configuration will be managed by the ICU.
- A routing table accessible via the configuration port which holds the logical address to output port mapping.
- Control logic to control the operation of the switch, performing arbitration and group adaptive routing.
- Control registers than can be written and read by the configuration port and which hold control information e.g. link operating speed.
- Internal status/error registers accessible via the configuration port.

The configuration port performs read and write operations to internal router registers (control and status). The routing table is set by the router command packets to assign logical addresses to physical destination ports on the router. When a packet is received with a logical address the routing table is checked by the routing control logic and the packet is routed to the destination port when the port is ready. The routing table logical addresses can also be set to support high priority and header deletion.

### 5.4.1.4.2.2 External Connectors

<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDM</td>
<td>9S</td>
<td>MEU/ICU Ifz</td>
<td>SpW Router</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>TEST Ifz</td>
<td>SpW Router</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TestBed</td>
</tr>
</tbody>
</table>

**SpW Router board External Connectors**

### 5.4.1.4.2.3 Internal Connectors

<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MHD</td>
<td>100P Interface with the Motherboard</td>
<td>SpW Router</td>
<td>Motherboard</td>
</tr>
</tbody>
</table>

**SpW Router board Internal Connectors**
Note: The signals in the MHD connector of the SpW Router board are mainly:

- SpW signals: to connect with the four N-DPUs, the PSU and the other Router.
- Secondary supply voltages for this board coming from the PSU.

5.4.1.4.2.4 Mechanical layout and budgets
The size of this board will be 100 x 220 mm. Next figure represents a layout of the board with the main components.

5.4.1.4.3 PSU board
The Power Supply Unit board performs two main tasks:
- Generates the Secondary Power Supply for the rest of the MEU boards from the Primary Power Supply Bus received from the platform.
- Switches ON or OFF the rest of the boards according to the TCs received from the ICUs.

5.4.1.4.3.1 Secondary Power Supply
The MEU Power Supply Unit will provide the overall voltages needed for the MEU subsystems. It will be based on a single board with 6 individual DC/DC converters, one for each N-DPU card and one powering each SpaceWire routers. This concept guarantees that if one converter fails, only one N-DPU, and therefore only 2 telescopes, will be lost. Each converter is capable of supplying the total power required for the operation of each of the MEU cards.

The converters will receive raw +28V input voltages from a single spacecraft power interface. The MEU-PSU will distribute the secondary voltages to each MEU subsystem (the 4 N-DPU boards and the 2 router units).
The MEU-PSU will include current sensing of each MEU sub-system.

The MEU-PSU is connected to the SpaceWire network. The analog housekeeping acquired by the PSU (current consumptions of each DPU board and each Router) will be sent to the ICU over the SpaceWire network.

5.4.1.4.3.2 Switching on / off

The MEU-PSU will include on/off controlled switches to power on/off independently each N-DPU board and each SpW Router board. The power on/off switching operation of the MEU subsystems (N-DPU boards, routers) are commanded by the ICU-M Processor Unit or by the ICU-R Processor Unit thanks to a SpaceWire command sent to the MEU-PSU.

The Router-M and the Router-R of each MEU work nominally in cold redundancy. At least one of the Router should be always ON to route the commands to the PSU. At power-on the PSU will supply power to both routers simultaneously, to guarantee the reception of TCs from both ICUs. The non-used Router will be immediately switched-off upon reception of the corresponding TC from the ICU. This strategy assures the reception of TCs from the ICU at switch-on, even if one of the SpW routers is not properly working.

5.4.1.4.3.3 Design Budgets

The PSU has to provide the voltages 1,2V; 1,5V; 1,8V; 2,5V; 3,3V to the other boards in the MEU (as detailed in next table).

<table>
<thead>
<tr>
<th>MEU Supply Voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Board</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>N-DPU</td>
</tr>
<tr>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>SpW Router</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

Note: The secondary distribution will be shared between the N-DPUs and PSU, some of the voltages could be produced in the N-DPU boards. Depending on voltages tolerances some of these values could be also simplified.

5.4.1.4.3.4 HW Implementation

The PSU for the PLATO MEU will be based on the PSU presently being developed for the Bepi Colombo MIXS instrument. This PSU is being manufactured by CRISA under contract and supervision.
by CAB-INTA. The MIXS PSU includes 1 converter to power the MIXS DPU, and 3 additional converters for the different detector units. The PLATO MEU PSU will consist on a set of input filters and 6 individual converters, one for each N-DPU card and one for each of the 2 Spacewire routers. These converters will be very similar to the MIXS DPU converter, with just some modifications to fit the voltage outputs required by the N-DPU cards (as explained above, the final voltages and tolerances for the N-DPU cards will be specified in the next phase of design). The MEU PSU board will include the 6 individual converters. We describe in this section the current design of the N-DPU/SpW router converter.

5.4.1.4.3.4.1 Input filters

At the PSU input, a set of filters will be included. To optimize the surface and weight budget, the input filters will be common to the 4 converters. In order to filter the common mode emission due to the current induced through the parasitic capacitors to chassis of the power switching devices, a common mode filter is mounted at the input of the converter. It consists of a high frequency filter at the input and a common mode filter. The inrush current limiter allows a soft switch ON of the converter by charging slowly the input filter capacitor, furthermore used with the inhibit circuit it allows the switch off of the unit. At the output of the inrush current limiter, after the common mode filter, an input differential mode filter network is connected in order to attenuate the differential conducted emissions.

The PSU core is based on several switching power converters which shall provide different isolated power outputs to the instrument subsystems. The command and monitoring acquisition is implemented also inside the PSU, by dedicated switching circuitry for each subsystem using external control signals from the ICU, and by conditioning and multiplexing the secondary voltages which will be provided to the ICU as housekeeping data.

The converter topology chosen aims the minimization of parts count and cost, mass and associated surface and volume, whilst keeping compliance with the functional and performance requirements. The selected topology is based on a flyback converter, with linear regulators with current limitation when required.

5.4.1.4.3.4.2 Input UVP

This circuit disables the converters operation, since it is common for all of them, when the input bus is lower than a minimum safe operation voltage. When the input voltage overpass a specified voltage level then the protection enable the start-up of the SpW “Auxiliary Power Supply” in order to start-up the SpW converters. For the DPU converters this signal will habituate them only if an ON Command is received from the ICU.

Once the input voltage drops below the minimum safe operation voltage the protection disable the “Auxiliary Power Supply” of all the converters hence switching them OFF.

5.4.1.4.3.4.3 Hiccup & APS

A “start-up linear regulator” has been implemented, powered from the input bus to deliver the needed energy to the primary control in order to start the flyback converters, which will generate other two insulated auxiliary supplies to self-power its own control circuitry (for regulation and efficiency reason). This “start-up linear regulator” remains stopped as long as the auxiliary power supply self-generated by the flyback converters stays over an under-voltage threshold.
In case of under-voltage of the regulated line, mainly due to output short circuit, the “start-up linear regulator” will start again allowing the flyback control to operate in current limitation. Due to the flyback thermal limitation this operation is time limited in order to avoid overheat of the flyback MOSFET, then after few tens of ms the APS and then the flyback is switched OFF for a bit more than 1 second, then the APS will start again, enabling the flyback. This process will be repeated indefinitely until either the flyback converter is turned off or the short circuit disappeared. This process is called “hiccup”.

5.4.1.4.3.4.4 Flyback Power Stage

The free running switching frequency of the flyback has been set to about 110 kHz in order to allow a synchronisation frequency of 130 kHz which is a very usual switching frequency for these type of converters. It is higher enough to get reasonable sizes of power magnets and capacitors and lower enough to avoid excessive switching losses and noise emissions. The power transformer has 5 insulated outputs (1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V – precise number and values TBC). The power transformer also has another regulated output that supplies the primary auxiliary circuitries. An additional output is used as an energy regenerative clamp.

5.4.1.4.3.4.5 Flyback Control Stage

The PWM1845 controller integrates the clock, the voltage control loop, a “precision” reference voltage, the current control Loop and limitation, the PWM Comparator, an under-voltage protection and one totem-pole output. Minimum external components are required.

5.4.1.4.3.4.6 Output Rectification Stage

It consists of a diode and a capacitor for each output. The aim is to rectify the signal from the transformer core.

5.4.1.4.3.4.7 Overcurrent Protection

This protection measures flyback’s primary input average current filtering the current measured by the current sensor and then compares this average value with an accurate reference. When the average input current surpasses the reference value, the flyback will be stopped and will enter in Hiccup-mode.

5.4.1.4.3.4.8 Overvoltage Protection

The flyback converter outputs are protected against overvoltage by a simple zener-driven transistor circuit. The trigger point is set to approximately 15% above the maximum worst-case value of the regulated flyback output voltage in order to ensure that it is not tripped off under nominal operating circumstances.

This protection actuates on the previous over current circuitry and then it will enter in the same way in Hiccup mode until the flyback converter is switched OFF.
5.4.1.4.3.4.9 Synchronisation Clock

The converters have to be synchronised to ensure the good operation of the whole PSU. The frequency has been set to 130 kHz.

EM model of the PSU card for the Bepi Colombo MIXS instrument, built by CRISA. This card includes 1 DPU converter and 3 additional converters for the detector units.

5.4.1.4.3.5 External Connectors

<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sub-D 9P</td>
<td>Power Supply Bus</td>
<td>PSU</td>
<td>Platform</td>
</tr>
</tbody>
</table>

**PSU board External Connectors**

5.4.1.4.3.6 Internal Connectors

<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MHD 100P</td>
<td>Interface with the Motherboard</td>
<td>PSU</td>
<td>Motherboard</td>
</tr>
</tbody>
</table>

*PSU board Internal Connectors*

**Note:** The signals in the MHD connector of the PSU board are mainly:

- SpW signals: to connect with the SpW Routers.
- Secondary supply voltages for the rest of the MEU boards.
5.4.1.4.3.7 Mechanical layout and budgets

The board will be implemented in a standard Extended Double Euro Card (233.35x220mm).

5.4.1.4.4 N_DPU board

For the N-DPU design, the LEON2 AT697F processor will be used (100 MHz / SDRAM controller). This micro will be in charge of running the S/W application to obtain the relevant scientific data from the images captured by the cameras and sent by the N-FEEs to the N-DPUs.

An ACTEL RTAX FPGA will be used to implement the interfaces to communicate the N-DPUs with the rest of the elements of the payload (the N-FEEs and the ICUs).

The figure below gives an overview of the architecture of a N-DPU board based on the LEON2 AT697F processor.

5.4.1.4.4.1 HW Implementation

Four main elements are distinguished in the architecture of this board:

- The AT697F microprocessor
- The SpW Interfaces module, implemented in an Actel RTAX 4000 FPGA
Spw Links

The memories (SDRAM, SRAM and PROM)

Next paragraphs give a brief description of these main elements of the N-DPU board.

5.4.1.4.4.1 AT697F microprocessor

The microprocessor selected to execute the application software in the N-DPU is the ATMEL AT697F processor. This micro fulfills all the requirements needed for this board. The maximum working frequency is 100 MHz, which is enough to comply with the CPU budget specified in paragraph 5.4.1.3.5.

The AT697F is a highly integrated, high-performance 32-bit RISC embedded processor based on the SPARC V8 architecture. The implementation is based on the European Space Agency (ESA) LEON2 fault tolerant model.

The AT697F contains an on-chip Integer Unit (IU), a Floating Point Unit (FPU), separate instruction and data caches, hardware multiplier and divider, interrupt controller, debug support unit with trace buffer, two 32-bit timers, Parallel and Serial interfaces, a Watchdog, a PCI Interface and a flexible Memory Controller. The design is highly testable with the support of a Debug Support Unit (DSU) and a boundary scan through JTAG interface.

The processor is manufactured using the Atmel 0.18 µm CMOS process. It has been especially designed for space, by implementing on-chip concurrent transient and permanent error detection and correction.

In the figure where is depicted the HW architecture of the N-DPU board (section 5.4.1.2.1), the AT697 micro processor block diagram is drawn detailing the main logical blocks. Next table lists the main features of the micro.

5.4.1.4.4.1.2 SpW Interfaces module

The interfaces between the microprocessor and the other modules of the MEU equipment are based in SpaceWire buses. As there are no commercial components able to perform all the tasks needed to allow the data flow inside the N-DPU board, a custom circuit is going to be designed. It has been estimated that the Actel RTAX 4000 FPGA is capable enough for this implementation.

In the N-DPU hardware architecture diagram the FPGA is shown with the main logical blocks of this Interfaces Module. The following paragraphs give a brief description of those blocks.

5.4.1.4.4.1.2.1 SpW Router

This block is in charge of sending the SpW packets to the intended recipient. The N-DPU board receives information from the N-FEEs and from the ICUs, it also generates some packets to other equipments. All this packets have to be correctly routed.

The various flows of data existing through the SpW Router module are:

- From the N-FEEs to the N-DPUs (Data Flow 1, painted in blue in the following figure):
  - Data images (to be stored in the SDRAM)
The SpW router will be able of routing all these SpW packets.

- From the N-DPUs to the N-FEEs (Data Flow 4):
  - Configuration telecommands
- From the ICUs to the N-DPUs (Data Flow 3):
  - Configuration telecommands
  - HK and status telemetries (of N-DPU and N-FEE boards)
- From different blocks inside the N-DPU (Data Flow 2):
  - Relevant application data from the mass memory (SDRAM) to the micro working memory (SRAM)

The SpW router will be able of routing all these SpW packets.
5.4.1.4.1.2.2 Images reception blocks (RMAP IPs target)

The row images received from the N-FEEs are routed to the RMAP target block. This module includes the RMAP protocol decoder in order of extracting the images encapsulated inside the SpW write packets.

This block will be implemented using a commercial VHDL IP. There are two different RMAP IPs in the market:

- The SpaceWire RMAP Interface IP developed by STAR-Dundee
- The GRSPW2 IP by Aeroflex Gaisler

Both IPs are suitable for the N-DPU block.

These IPs receive the SpW packets, decode them, extract the information and send them to an AMBA AHB interface. The IPs act as bus masters. They also include some FIFO memories in order to store the packets while the bus is busy.

Four RMAP target blocks have to be included in the FPGA, one for each SpW link with the N-FEEs (there are two N-FEEs connected with the N-DPU, and two links at 100 Mbps for each N-DPU / N-FEE connection).

5.4.1.4.1.2.3 AMBA AHB Bus

The AMBA AHB bus will connect the RMAP target blocks with the memory controller.

The AMBA Advanced High-performance Bus (AHB) is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation. It implements the features required for high-performance, high clock frequency systems including:

- burst transfers
- split transactions
- single-cycle bus master handover
- single-clock edge operation
- non-tristate implementation
- wider data bus configurations (64/128 bits).

The AMBA AHB system design will contain the following components:

**AHB master** A bus master is able to initiate read and write operations by providing an address and control information. In the N-DPU board the AMBA AHB design will contain four bus masters, for the Direct Memory Access (DMA) to the SDRAM from the four SpW links that interface the two N-FEEs with the N-DPU. Only one of them is allowed to actively use the bus at any one time.

**AHB slave** A bus slave responds to a read or write operation within a given address-space range. The bus slave signals back to the active master the success, failure or waiting of the data transfer. In the N-DPU implementation, the external memory interface of the SDRAM will be the AHB slave.
**AHB arbiter** The bus arbiter ensures that only one bus master at a time is allowed to initiate data transfers.

**AHB decoder** The AHB decoder is used to decode the address of each transfer and provide a select signal for the slave that is involved in the transfer. In the N-DPU board, as there is only one slave, the decoder will be very simple.

The N-DPU will receive 4 SpW links at 100 Mbps, what means 400 Mbps of data. Besides, the packets in the 4 links arrive at the same time due to the synchronisation in the images sending procedure. So, the four DMA masters will try to give the packets to the AMBA bus at the same time. Only one of them will obtain the permission to use it. The other three has to store the packet temporally in the RMAP IP FIFOs. Before the first four packets are totally written in the SDRAM a new group of four packets could arrive, so the FIFO of each RMAP IP has to be dimension to store two RMAP packets.

Typical frequencies for the AMBA AHB bus are 33MHz or 40 MHz, which are enough to take out the first four packets of the FIFOs before the third group of packets comes, considering a data bus length of 32 bits.

5.4.1.4.4.1.2.4 Memories Controller

The Memories Controller will be the slave of the AMBA bus. This module is in charge of generate the control signals to write the data from the RMAP target blocks in the mass storage memory.

Once the images are written in the SDRAM, a second phase starts. In this stage the relevant information for the scientific application that will run in the AT697 microprocessor is read from the SDRAM again and written in the SRAM, which is the micro working memory. The Memories controller is in charge of executing the read and write process in the two memories.

5.4.1.4.4.1.2.5 RMAP IP Initiator and target

This block generates the packets to be sent to the N-FFE or the ICU. Three kind packets are going to be transmitted by the N-DPU:

- Packets with scientific results to the ICU. These packets are not generated according the RMAP protocol, the RMAP encoder module in the RMAP IP has to be disabled in this case.
- Packets with HK and status telemetries from the N-DPU to the ICU. These are RMAP packets.
- Packets with configuration parameters from the N-DPU to the N-FEEs. Also produced considering the RMAP protocol.

The micro is the master of this communications. It generates the information and the RMAP initiator IP is able to format the SpW packets according to the RMAP protocol if it is needed and address them to their destination.
5.4.1.4.1.4.1.2.6 Synchro and Control Module

This block comprises the control and synchronisation signals and procedures to ensure the correct behaviour of all the processes inside the N-DPU. In fact, this block is only conceptual, in the real design the control and synchronisation functions will be distributed in various blocks.

5.4.1.4.4.1.3 SpW Links

The SpaceWire buses are compliant with the standard ECSS-E-ST-50-12C. The hardware to implement the SpW links in the N-DPU is the same that in the SpW Router board. In paragraph 5.4.1.2.1.1 is written a brief description of the main components. For further details refer to the standard.

5.4.1.4.4.1.4 Memories

The N-DPU board includes three different kinds of memories: SDRAM, SRAM and PROM. They differ in the technology but also in the function they perform in the board.

5.4.1.4.4.1.4.1 SDRAM

The SDRAM is the “Mass storage” memory. It will store the images coming from the N-FEEs. Each N-DPU has to store two full images, coming from the two cameras connected to this board, before processing them. Also the SDRAM is used to save data processing parameters and to buffer the obtained information before send them to the ICU.

This memory needs to have a size of 256 Mbytes. In paragraph 5.4.2.3.6 a summary of the data to be stored in the SDRAM is shown.

5.4.1.4.4.1.4.2 SRAM

The SRAM will be used for the boot and the scientific applications execution. It needs space enough to keep software data and variables. An estimation of 32 Mbytes storage is done for this memory.

5.4.1.4.4.1.4.3 PROM

The PROM memory will contain the boot software. The size of this memory is TBD.

Note: An alternative proposal is that the ICU application software could be able of starting the N-DPU application through the processor DSU interface. In this case the PROM memory won't be included in the N-DPU board.
5.4.1.4.4.2 External Connectors

<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM MEU</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDM</td>
<td>9S N-DPU/N-FEE1 Itfz 1</td>
<td>N-DPU</td>
<td>N-FEE1</td>
</tr>
<tr>
<td>MDM</td>
<td>9S N-DPU/N-FEE1 Itfz 2</td>
<td>N-DPU</td>
<td>N-FEE1</td>
</tr>
<tr>
<td>MDM</td>
<td>9S N-DPU/N-FEE2 Itfz 1</td>
<td>N-DPU</td>
<td>N-FEE2</td>
</tr>
<tr>
<td>MDM</td>
<td>9S N-DPU/N-FEE2 Itfz 2</td>
<td>N-DPU</td>
<td>N-FEE2</td>
</tr>
</tbody>
</table>

N-DPU board External Connectors

5.4.1.4.3 Internal Connectors

<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MHD</td>
<td>100P Interface with the Motherboard</td>
<td>N-DPU</td>
<td>Motherboard</td>
</tr>
</tbody>
</table>

N-DPU board Internal Connectors

Note: The signals in the MHD connector of the N-DPU board are mainly:
- SpW signals: to connect with the SpW Routers.
- Secondary supply voltages for this board coming from the PSU.

5.4.1.4.4 Mechanical layout and budgets

The board will be implemented in a standard Extended Single Euro Card (100x220mm).
5.4.1.5 MEU PHYSICAL IMPLEMENTATION

The MEU consists of four different boards:

- N-DPU Board
- SpaceWire Router Board
- PSU Board
- Mother Board

The main board is the N-DPU which is in charge of processing the images coming from two N-FEEs. Each MEU processes the images from eight N-FEEs so four N-DPU boards are included in each MEU box.

Also the SpaceWire Routers are redounded in order of increasing the reliability of the equipment. In the normal operation mode they work in cold redundancy, but in for exceptional cases hot redundancy would be also possible.

So a final number of eight boards are included in the MEU box. The interconnection of the boards is made by means of a Mother Board, on the back side of the equipment and perpendicular to them, with seven slots to place the boards. All the external connectors of the MEU will be located in the boards in the opposite side of the Motherboard (the front or connectors side).

The total list of boards included within one MEU box is the following:

- N-DPU 1
- N-DPU 2
- N-DPU 3
- N-DPU 4
- SpaceWire Router Main
- SpaceWire Router Redundant
- Power Supply Unit
- Mother board

Boards are fixed to the structure by means of wedge-lock guides, joining them rigidly to the structure. Front cover performs mechanical interface between connectors and structure. Once all boards are fixed in the structure, they will be torqued by means of guide’s screws. Back cover is the last part to be assembled fixing the back side of board structures to the whole equipment.

Feet are located at the bottom structure machined on it allowing guides thermal mechanical transmission through them. Laterals improve thermal behaviour supplying good thermal path to the platform.

In order to allow good electrical path between equipment and the platform, the equipment finished will be chromate with ALODINE 1200.

The next figure shows the equipment assembly concept.
5.4.1.5.1 Equipment Connectors

External connectors are located on front side of the equipment. Connections of the rear side of the boards (internal connections) will be made via motherboard, and connections of the front side will be made directly from each board.

Straight pin solder contacts will be used for motherboard's connectors, and right angle pin solder contacts for the other boards of the equipment.

5.4.1.5.1.1 External Connectors

MDM 9 pin female connectors will be used for external SpaceWire links. For primary supply Sub-D (TBC) connector will be used. These connectors are mounted on the front sides of the boards, and are externally fixed to the structure by means of screw locks.

The proposed connectors of the unit will be:
<table>
<thead>
<tr>
<th>TYPE</th>
<th>FUNCTION</th>
<th>FROM MEU</th>
<th>TO</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDM</td>
<td>9S</td>
<td>SpW ICU-M</td>
<td>SpW Router-M</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>SpW ICU-M</td>
<td>SpW Router-M</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>SpW ICU-R</td>
<td>SpW Router-R</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>SpW ICU-R</td>
<td>SpW Router-R</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>N-DPU1/N-FEE1 Itfz 1</td>
<td>N-DPU2</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>N-DPU1/N-FEE1 Itfz 2</td>
<td>N-DPU3</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>N-DPU2/N-FEE1 Itfz 1</td>
<td>N-DPU4</td>
</tr>
<tr>
<td>MDM</td>
<td>9S</td>
<td>N-DPU2/N-FEE1 Itfz 2</td>
<td>N-DPU5</td>
</tr>
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<td>9S</td>
<td>N-DPU1/N-FEE2 Itfz 1</td>
<td>N-DPU6</td>
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<td>N-DPU1/N-FEE2 Itfz 2</td>
<td>N-DPU7</td>
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<td>9S</td>
<td>N-DPU3/N-FEE1 Itfz 1</td>
<td>N-DPU8</td>
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<tr>
<td>MDM</td>
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<td>N-DPU3/N-FEE1 Itfz 2</td>
<td>N-DPU9</td>
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<td>9S</td>
<td>N-DPU4/N-FEE1 Itfz 1</td>
<td>N-DPU10</td>
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<tr>
<td>MDM</td>
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<td>N-DPU4/N-FEE1 Itfz 2</td>
<td>N-DPU11</td>
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<tr>
<td>MDM</td>
<td>9S</td>
<td>N-DPU5/N-FEE1 Itfz 1</td>
<td>N-DPU12</td>
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<tr>
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<td>9S</td>
<td>N-DPU5/N-FEE1 Itfz 2</td>
<td>N-DPU13</td>
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<td>MDM</td>
<td>9S</td>
<td>N-DPU6/N-FEE1 Itfz 1</td>
<td>N-DPU14</td>
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<tr>
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<td>9S</td>
<td>N-DPU6/N-FEE1 Itfz 2</td>
<td>N-DPU15</td>
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<tr>
<td>MDM</td>
<td>9S</td>
<td>N-DPU7/N-FEE1 Itfz 1</td>
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<td>N-DPU7/N-FEE1 Itfz 2</td>
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<td>9S</td>
<td>N-DPU8/N-FEE1 Itfz 1</td>
<td>N-DPU18</td>
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<td>9S</td>
<td>N-DPU8/N-FEE1 Itfz 2</td>
<td>N-DPU19</td>
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<td>9S</td>
<td>N-DPU9/N-FEE1 Itfz 1</td>
<td>N-DPU20</td>
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<td>9S</td>
<td>N-DPU9/N-FEE1 Itfz 2</td>
<td>N-DPU21</td>
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<tr>
<td>Sub-D</td>
<td>9P</td>
<td>Platform</td>
<td>PSU</td>
</tr>
</tbody>
</table>

*MEU external connectors table*
5.4.1.5.1.2 Internal Connectors

MHD connectors of 100 pins (TBC) will be used for internal connections between N-DPUs, SpaceWire Router and PSU boards (through the Motherboard). They are female connectors in the Motherboard side and male in the other boards.

The internal connectors are used to distribute two groups of signals:

- Secondary power supply signals: From PSU to the N-DPUs and the SpaceWire Routers.
- Internal SpaceWire links: Between the SpaceWire Routers and the N-DPUs and the PSU.

5.4.1.6 MEU BUDGETS

5.4.1.6.1 Power budgets

In this section an overview of the MEU power consumption is provided. All information shall be structured in the form of tables to show the different contributions to the overall figure. The power consumptions are estimated according the maximum consumption of all the components included in
each board specified in the corresponding Data Sheets. So this budget should be considered as a Worst Case. The typical values are expected to be smaller.

5.4.1.6.1.1 N-DPU Maximum Power Consumption

<table>
<thead>
<tr>
<th>Component Name</th>
<th>Power/Unit (W)</th>
<th>Nr Of Units</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA RTAX 4000</td>
<td>4.00</td>
<td>1</td>
<td>4.00</td>
</tr>
<tr>
<td>AT697F LEON 2</td>
<td>1.00</td>
<td>1</td>
<td>1.00</td>
</tr>
<tr>
<td>SDRAM</td>
<td>1.80</td>
<td>1</td>
<td>1.80</td>
</tr>
<tr>
<td>PROM</td>
<td>0.55</td>
<td>1</td>
<td>0.55</td>
</tr>
<tr>
<td>SRAM</td>
<td>0.50</td>
<td>1</td>
<td>0.50</td>
</tr>
<tr>
<td>SpW Transceivers</td>
<td>0.05</td>
<td>6</td>
<td>0.30</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>8.15</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**N-DPU Maximum Power Consumption**

5.4.1.6.1.2 SpaceWire Router Maximum Power Consumption

The consumption of the AT7910F ASIC is estimated with the formula:

\[
\text{AT7910F Maximum Power Consumption} = \text{Pop} - ((\text{Pop-Poff}) \times 0.1 + 0.06) \times \text{NrOfSpWDisabled}
\]

Next table summarises the Maximum Power Consumption of the ASIC according to the parameters applicable to the SpW Router board in the MEU equipment:

<table>
<thead>
<tr>
<th>Component Name</th>
<th>Power/Unit (W)</th>
<th>NrOfSpWDisabled</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT7910F ASIC</td>
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<td>2.00</td>
<td>2.12</td>
</tr>
<tr>
<td>SpW Transceivers</td>
<td>0.05</td>
<td>6.00</td>
<td>0.30</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>2.42</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**AT7910F Maximum Power Consumption**

*Note:* Tests SpaceWire ports are not active in normal operation mode \((\text{NrOfSpWDisabled} = 2)\).

The overall power estimation of the SpaceWire Router boards includes the SpaceWire drivers and receivers:

<table>
<thead>
<tr>
<th>Component Name</th>
<th>Power/Unit (W)</th>
<th>Nr Of Units</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT7910F ASIC</td>
<td>2.12</td>
<td>1.00</td>
<td>2.12</td>
</tr>
<tr>
<td>SpW Transceivers</td>
<td>0.05</td>
<td>6.00</td>
<td>0.30</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td><strong>2.42</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SpaceWire Router Maximum Power Consumption

Note: Only one SpaceWire Router is active in normal operation mode.

5.4.1.6.1.3 PSU DC/DC efficiency
For the PSU an efficiency of 80\% has been considered.

5.4.1.6.1.4 MEU Maximum Power Consumption

<table>
<thead>
<tr>
<th>Board Name</th>
<th>Power/Unit (W)</th>
<th>Nr of Units</th>
<th>Power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SpW Router</td>
<td>2.42</td>
<td>1</td>
<td>2.42</td>
</tr>
<tr>
<td>N-DPU</td>
<td>8.15</td>
<td>4</td>
<td>32.60</td>
</tr>
<tr>
<td>Total without efficiency</td>
<td></td>
<td></td>
<td>35.02</td>
</tr>
<tr>
<td>PSU efficiency</td>
<td>0.80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TOTAL with efficiency</td>
<td></td>
<td></td>
<td>43.78</td>
</tr>
</tbody>
</table>

MEU Maximum Power Consumption

5.4.1.6.2 Mass Budget
The mass budget is summarised in the next table.

<table>
<thead>
<tr>
<th>MEU Equipment</th>
<th>N° Items</th>
<th>Weight per Item</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-DPU board</td>
<td>4</td>
<td>380</td>
<td>1520</td>
</tr>
<tr>
<td>SpW Router Board</td>
<td>2</td>
<td>340</td>
<td>680</td>
</tr>
<tr>
<td>PSU board</td>
<td>1</td>
<td>800</td>
<td>800</td>
</tr>
<tr>
<td>Motherboard</td>
<td>1</td>
<td>500</td>
<td>500</td>
</tr>
<tr>
<td>Mechanical Equipment</td>
<td>1</td>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4500</td>
</tr>
</tbody>
</table>

Mass Budget

5.4.1.6.3 Dimension Budget
The MEU box has an estimated dimension of 160 mm (X) x 295 mm (Y) x 250 mm (Z).

Next table includes the size of all the boards in the box.

<table>
<thead>
<tr>
<th>MEU Equipment</th>
<th>Board Type</th>
<th>Number of Boards</th>
<th>Dimension (mmxmm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-DPU board</td>
<td>Extended Single Euro Card</td>
<td>4</td>
<td>100x220</td>
</tr>
<tr>
<td>SpW Router Board</td>
<td>Extended Single Euro Card</td>
<td>2</td>
<td>100x220</td>
</tr>
<tr>
<td>PSU board</td>
<td>Extended Double Euro Card</td>
<td>1</td>
<td>233.35x220</td>
</tr>
<tr>
<td>Motherboard</td>
<td>No standard</td>
<td>1</td>
<td>233.35x130</td>
</tr>
</tbody>
</table>

Boards Dimensions
The preliminary ICD of the MEU box is depicted below.

**NOTE:** The box could be oriented in the direction that better fits with the space in the satellite, the axis X, Y, Z in the figure below could be rotated.

---

**Preliminary ICD**

### 5.4.2 FEU

This section gives an overview of the FEU design including hardware, software and data processing.

#### 5.4.2.1 REQUIREMENTS

##### 5.4.2.1.1 Common requirements

See section 5.4.1.5: N-DPU (same requirements).
5.4.2.1.2 Observation mode requirements

The processing of each exposure is done in five steps: 1) Full-frame image acquisition, 2) Window extraction, 3) Data correction and reduction, 4) Angle error measurement, 5) Mask and star position updating.

The requirements for the steps 1), 2), 3) and 5) are identical to the ones given for the N-DPU except for the points below:

- The distribution of the extracted windows is the following (count for the 4 CCDs):
  
<table>
<thead>
<tr>
<th>Window Type</th>
<th>Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stars</td>
<td>400</td>
</tr>
<tr>
<td>Background windows</td>
<td>100</td>
</tr>
<tr>
<td>Imagettes</td>
<td>40</td>
</tr>
<tr>
<td>Offset windows</td>
<td>2 x 4 offset windows</td>
</tr>
<tr>
<td>Smearing rows</td>
<td>4 x 10 overscan rows</td>
</tr>
</tbody>
</table>

- The size of the windows is about 7x7 pixels (TBC).
- The cadence of the data correction and reduction process is 2.5 sec instead of 25 sec.
- The photometric algorithms will be based on the optimal mask method which gives the best results for the fast camera configuration (TBC).
- The FGS algorithms are based on an extended Kalman filter (EKF) used for recursive nonlinear optimization
- The FEU shall perform angle error measurements which are provided to the platform AOCS, also called Fine Guidance System (FGS). The noise contribution to the pointing accuracy or stability of the whole satellite controlled by AOCS is expected to be better than 0.032 arcsec/√Hz.

5.4.2.2 HARDWARE DESIGN

5.4.2.2.1 Flow rates to the FEE

The Pixels are digitalized at a rate of 4 Mpixel/sec thus the max rate per half CCD is 64 Mbps. With 8 links (one per half CCD output), including the spaceWire overhead, it gives 80 Mbps as a peak rate. In order to cope with this bit rate with margin, the link should be configured at 100 Mbps for 8 links or 200 Mbps for 4 links.

The mean rate is 1.25 (SpW overhead) * image size / 1.5 (readout time) so it is: 1.25 * 81 / 1.5 = 68 Mbps and it gives 30 % margin.

5.4.2.2.2 Processing power

The computation power is calculated based on calculations and measurements done for FGS algorithms, science data processing as done for the normal DPU, but adapted to the limited star number including the computation power for the angle error calculation. The computation resources is calculated for all processing steps performed during a typical operation scenario (400 stars, 100 Backgrounds, 40 Imagettes, 2 x 4 Offset Windows, 4x10 Overscan Rows within 2.5s).
The CPU load needed by the data acquisition, correction and reduction process is about 40% with a MDPA LEON2 FT processor running at 80 MHz. A computing power better than 0.81 Dhrystone MIPS/MHz or 65 Dhrystone MIPS is assumed.

The following table gives an estimation of instructions for the different processing steps:

<table>
<thead>
<tr>
<th>Processing step</th>
<th>Instructions</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Window extraction</td>
<td>10.2 E+06</td>
<td>1526 * 1.36 * (400 Stars + 100 Background) +</td>
</tr>
<tr>
<td></td>
<td></td>
<td>751 * 1.36 * 40 Imagettes +</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500,000 (Offset) +</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8,600.00 (Smearing)</td>
</tr>
<tr>
<td>Data correction and reduction</td>
<td>45 E+06</td>
<td>(3105 + 3226) * 1.36 * 400 Stars +</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10,876 * 1.36 * 100 Background +</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2,900,000 (Offset) +</td>
</tr>
<tr>
<td></td>
<td></td>
<td>37,200,000 (Smearing)</td>
</tr>
<tr>
<td>Angle error measurement</td>
<td>9.3 E+06</td>
<td>Measured with a Leon3 FT@50MHz target</td>
</tr>
<tr>
<td>Mask and Star position update</td>
<td>0.1 E+06</td>
<td>estimated</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>64.6 E+06</strong></td>
</tr>
</tbody>
</table>

**Calculation of data processing cycles**

The values are based on RD1 and are scaled to the F-DPU window size with a factor of 1.36. As calculated the F-DPU shall execute 64.6 E06 instruction in a frame period of 2.5s or 25.76 E06 instructions per second. With the LEON2 FT@80MHz computing power of 65 MIPS we expect a duty cycle of less than 39.6%. This value doesn’t include the TM Transfer and the RTOS overhead. But this will be less than 10% incl. margin.

Summarized, the calculated CPU load for a LEON2 FT@80MHz is less than 50%.

**5.4.2.2.3 Memory usage**

The memory size needed at runtime is summarized as follows:

- PBS code size: < 28 kbyte (incl. compression, to be stored in PROM)
- APS code size incl. RTEMS: < 310 kByte (to be stored in EEPROM)
- Small start catalog: < 400 kByte (to be stored in EEPROM)
- Data memory size: < 3800 kByte (SRAM)

The PBS size calculation is based on already existing software developed for BepiColombo/MERTIS.

The data memory size is calculated including the memory usage for the code, intermediate data processing, RTEMS usage incl. stack and TM/TC data buffering.

**5.4.2.2.4 Hardware architecture**

The FEU is an integrated electronics box. The unit consists of:
• 2 data processing (F-DPU) boards (each within one module frame) and
• 2 power converters (PSU) integrated into a single frame.

The FEU receives main power from the spacecraft. The PSU generates all internal secondary voltages for the F-DPU boards. No secondary voltages are supplied to external units.

The hardware functions of the FEU are:

• Provide Command and Control Interface for the F-FEE via 8 SpaceWire Links and Remote Memory Access Protocol (RMAP)
• Provide acquisition means for image data from the F-FEE via the same 8 SpaceWire Links and Remote Memory Access Protocol (RMAP)
• Store the received image in FEU internal SDRAM memory
• Provide SW Processor for running the application software (APS)
• Provide SRAM memory for APS data/program
• Provide EEPROM memory for APS program
• Proved PROM for primary boot software (PBS)
• Provide internal housekeeping values available for the APS

The figure below gives an overview of the FEU box architecture.

Reference Example for FEU mechanical layout

5.4.2.2.5 Electrical Interfaces

The table below summarizes the external and internal module interfaces:
### Interfaces for one F-DPU module

<table>
<thead>
<tr>
<th>I/F</th>
<th>Interface</th>
<th>Type</th>
<th>Qty</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEU-SVM</td>
<td>AOCS Link</td>
<td>Mil1553B</td>
<td>2</td>
<td>(main+red.)</td>
</tr>
<tr>
<td>FEU-ICU</td>
<td>TM/TC and Time</td>
<td>SpaceWire</td>
<td>2</td>
<td>(main+red.)</td>
</tr>
<tr>
<td>FEU-FEE</td>
<td>F-FEE SpaceWire</td>
<td>SpaceWire</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>EGSE</td>
<td>Technological_#1 DSU-SPW, DSU-UART</td>
<td>SpaceWire RS-422</td>
<td>1</td>
<td>only for ground use</td>
</tr>
<tr>
<td>EGSE</td>
<td>Service Interface (SIF)</td>
<td>SpaceWire</td>
<td>1</td>
<td>only for ground use</td>
</tr>
<tr>
<td>Internal</td>
<td>Supply Rail F-DPU Core (Incl. Returns and Sense)</td>
<td>1_8V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Internal</td>
<td>Supply Rail F-DPU (Incl. Returns and Sense)</td>
<td>3_3V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Internal</td>
<td>Supply Rail MilBus/HK (Incl. Returns and Sense)</td>
<td>15V (TBC)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Internal</td>
<td>Analogue HK</td>
<td>analogue</td>
<td>8</td>
<td>number of HK is TBC</td>
</tr>
</tbody>
</table>

### Interfaces for one PSU

<table>
<thead>
<tr>
<th>Ext/Int</th>
<th>Interface</th>
<th>Type</th>
<th>Qty</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>FEU-SVM</td>
<td>Power Input</td>
<td>28V regulated</td>
<td>2</td>
<td>No redundant PDU on SVM, only one power I/F from SVM to each F-DPU-PSU</td>
</tr>
<tr>
<td>FEU-SVM</td>
<td>Status</td>
<td>RSA (TBC)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>FEU-SVM</td>
<td>Switch_On_Off</td>
<td>HPC (TBC)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Internal</td>
<td>Supply Rail F-DPU Core (Incl. Returns and Sense)</td>
<td>1_8V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Internal</td>
<td>Supply Rail F-DPU (Incl. Returns and Sense)</td>
<td>3_3V</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Internal</td>
<td>Supply Rail MilBus/HK (Incl. Returns and Sense)</td>
<td>15V (TBC)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Internal</td>
<td>ANA HK</td>
<td>analogue</td>
<td>8</td>
<td>number of HK is TBC</td>
</tr>
</tbody>
</table>
FEU Architecture Block Diagram
5.4.2.2.6 Data Processing Module (F-DPU)

5.4.2.2.7 F-DPU Architecture

A detailed architectural block diagram is shown in the next figure.

Two main components reside on the board, the MDPA ASIC and one FPGA (Actel RTAX2000 tbc).

All external interfaces, except the F-FEE interface, are handled by the MDPA ASIC. For the PLATO FEU, those interfaces are: the ICU interface implemented as a redundant SpaceWire type and the AOCS/SVM interface implemented as redundant MilStd 1553B Remote Terminal (RT) type.

The Leon2FT processor accesses all peripherals via the MDPA internal AHB bus architecture. An integrated AHB memory controller gives access to external memories and to the external SDRAM memory controller implemented in the FPGA. Additionally or alternatively, the SDRAM can be accessed via an internal SpaceWire link with the help of the SpaceWire DMA capability. The processor runs with up to 80 MHz and

The dedicated F-DPU FPGA (Actel RTAX type) handles the fast acquisition of the CCD image input by means of 8 SpaceWire interfaces and stores the input data in SDRAM. The baseline protocol for the memory access is RMAP. The transfer of a half CCD line (corresponds to one FEE SpaceWire Link) is made by means of one RMAP write command in non-acknowledged / non-verified mode to allow continues and uninterrupted transmission. Thus, the F-FEE is responsible for correct addressing the SDRAM memory via the RMAP protocol. The link speed is 100MBit/s which gives sufficient margin for the maximum net data rate of 64MBit/s. The FEU design would be capable of data rates up to 200MBit/s. Further functions are implemented as follows:

SDRAM controller for single data rate SDRAM types: The SDRAM data bus is 64 bit and the SDRAM clock is 40MHz. The theoretical maximum burst data rate is therewith <2560MBit/s. The realistic data rate (including e.g. SDRAM command overhead) offers still sufficient margin to receive the incoming data (8x100MBit/s max) and to provide arbitrary read access by the SW.

An IO controller: to connect the FPGA with the MDPA and to map the SDRAM memory logically into the AHB addresses space. In order to handle the access, a bus ready signal is used to add wait states.

The FEE command and control logic: By means of RMAP write and read commands the FEE is accessible from the FEU. The MDPA SW has access to dedicated registers in the FPGA to send TC and receive TM from the FEE.

An HK controller: analogue housekeeping data is acquired by the FPGA from an multi-channel ADC in order to provide FEU status of voltage and currents of the secondary supply.

Some glue logic (address decoding, EEPROM power-up sequence) to save discrete components.
FEU - Data Processing Module Architecture
5.4.2.2.8 MPDA ASIC

The MDPA ASIC is intended to be the processor for the F-DPU. This chip was developed by EADS Astrium GmbH using the 0.18um ATC18 ASIC radiation tolerant technology from the European manufacturer Atmel. It is packaged in MQFP-352 case. The ASIC offers processing capability of up to 70MIPS and all needed interfaces for the F-DPU such as: 8 SpaceWire Links, EEPROM/PROM and SRAM controller. The processor can be booted via SpaceWire RMAP from the ICU if needed, thus saving the boot PROM/EEPROM. Although the baseline is that the F-DPU will be equipped with PROM/EEPROM in order to provide a self-standing unit. Some key features of the MDPA are listed hereafter:

- LEON2-FT, based on SPARC V8 RISC 32bits architecture
- Operating Frequency up to 80 MHz
- 16Kbyte Data Cache, 32Kbyte Instruction Cache
- Floating Point unit: Meiko FPU, 32bits IEEE 754

5.4.2.2.9 FPGA

The FPGA implementation is foreseen in a Rad-Tolerant Actel/Microsemi RTAX2000 FPGA. A first assessment of the pin count has been done to determine the needed FPGA package.

<table>
<thead>
<tr>
<th>Name</th>
<th>Pins</th>
<th>Qty</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>F-FEE SpW</td>
<td>4</td>
<td>8</td>
<td>32</td>
</tr>
<tr>
<td>SDRAM Data</td>
<td>64</td>
<td>1</td>
<td>64</td>
</tr>
<tr>
<td>SDRAM EDAC</td>
<td>8</td>
<td>1</td>
<td>8</td>
</tr>
<tr>
<td>SDRAM Addr</td>
<td>17</td>
<td>1</td>
<td>17</td>
</tr>
<tr>
<td>SDRAM Control</td>
<td>5</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>IO Data</td>
<td>32</td>
<td>1</td>
<td>32</td>
</tr>
<tr>
<td>IO Addr</td>
<td>28</td>
<td>1</td>
<td>28</td>
</tr>
<tr>
<td>IO Control</td>
<td>4</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>Control Spw</td>
<td>4</td>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>HK ADC SPI</td>
<td>3</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>Glue Logic</td>
<td>12</td>
<td>1</td>
<td>12</td>
</tr>
<tr>
<td>Reset</td>
<td>2</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Clock</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Total** 212

*Needed IO of FPGA*

The total number of IO pins show that probably a CGA624 package is needed.

A first assessment of needed Gate Resources has been performed. It can be shown that the available resources of an AX2000 FPGA are very likely sufficient; roughly 62% of sequential and 40% of combinatorial elements are needed.
For the SpW implementation an ECSS compliant SpaceWire IP core will be used. Special attention has to be drawn on the proper implementation of the SpaceWire RX clock recovery mechanism, as this circuit is working asynchronously. Thus, regular synthesis and FPGA tools need to be handled in a special way. As every SpaceWire cell has at least 2 clocks (rx clock, tx clock), a minimum of 20 clock nets are needed for the 10 SpaceWire cells. To cope with this, the special clock segmentation features of the Actel AX family can be deployed.

5.4.2.2.10 Memory

The size of the on-board memory is dependent on the needed resources for:

- Primary Boot Software (PBS)
- Application Software (APS) and parameter
- Small Star Catalogue
- Size of image buffer.

With respect to the image buffer, one complete image comprises 4x2253x4510x16bit = 650MBit ~ 82 MByte. A few images must be stored in the FEU for further processing.

Therefore it is foreseen to provide 512MByte of SDRAM memory. This allows storing 6 complete images.

With respect to the other memory sizes, values typical for PBS and APS have been considered.

The proposed memory usage approach and sizes is summarized in the table below:

<table>
<thead>
<tr>
<th>Memory</th>
<th>Size on F-DPU</th>
<th>Used for</th>
<th>Estimated Need</th>
</tr>
</thead>
</table>
SRAM and SDRAM are EDAC protected for single bit error correction and double bit error detection.

5.4.2.2.11 Power Supply Unit (PSU)

The Power Supply module comprises the DC/DC converters to generate the FEU internal supply voltages.

The PSU development will be mainly based on a recurrent space-qualified design concept applicable for a wide range of input voltages (16V - 60V) which will be adapted to the PLATO needs (28V regulated bus).

The primary power input is non-redundant and of 28V (regulated or unregulated) type.

The secondary voltages are:

- 3.3V for digital logic, MDPA and FPGA IO voltage
- 1.8V for MDPA core
- 1.5V for FPGA core

The PSU architecture comprises:

- an input stage with EMI Filter, inrush current limiter and overcurrent / overvoltage protection
- a DC/DC to provide galvanically isolation and a PWM regulation to generate 3.3V secondary voltage
- Linear Regulator to generated 1.8/1.5V secondary.

The converter efficiency is at least 75%.

5.4.2.2.12 Key Components

The preliminary selection of key components has been performed. In some cases, alternative components have been identified and the final selection must be done after thorough trade-off regarding functions, packages, availability, risks etc. It is clearly understood, that in order to guarantee the needed quality, reliability and radiation performance only space-qualified components are candidates.
5.4.2.2.13 Reliability

A preliminary reliability assessment has been performed on the basis of an existing similar unit. It results in the following reliability figures:

F-DPU Module: 800 FIT
Converter Module: 280 FIT

A lifetime of 8 years and component level QML-V is assumed.

The resulting total reliability is approximately 99.5 % for the hot redundant unit.

5.4.2.2.14 Radiation Tolerance

Several means to withstand and tolerate single-event-effects (SEE) such as SEU, SEL, SET are taken into account of the hardware design.

The following table lists the potential candidates for SEE and shows the mitigation measures.
<table>
<thead>
<tr>
<th>Device</th>
<th>Function / Device Property</th>
<th>Correction Mechanism</th>
<th>SW interaction / operational degradation</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDPA Register File RAM</td>
<td>Processor Register File RAM</td>
<td>EDAC (1 bit correction) with automatic re-write function</td>
<td>Error counter increments No performance degradation</td>
</tr>
<tr>
<td>EEPROM MMEE08001808S-C (TBC)</td>
<td>Non-volatile Application SW storage Only powered during boot and image upload</td>
<td>CRC protected (1 or more bit errors detection)</td>
<td>Minor performance Degradation</td>
</tr>
<tr>
<td>SRAM AT60142F15/AT68166F (TBC)</td>
<td>Program/data/EDAC Memory Cells of same word are physically separated</td>
<td>EDAC protection (1 bit correction)</td>
<td>AHB interrupt on respective read access of address location; address location need to be re-written; minor performance degradation</td>
</tr>
<tr>
<td>SDRAM</td>
<td>Intermediate Storage of Image for Processing</td>
<td>EDAC foreseen (one bit correction in 64bit word) SEL detection against permanent damage due to latch-up (TBC)</td>
<td>Auto correction for single bit error, Corruption of image pixel(s) if &gt;1 bit error SEL - SW interrupt, re switch-on SDRAM device, loss of image</td>
</tr>
</tbody>
</table>

**SEE effect and countermeasures**

In case of an unlikely event of SEU in the CPU or SET in the clock tree, the CPU malfunction would lead to an error trap or software independent watchdog timeout. The first timeout leads to SW interrupt, second level lead to a warm reset.

### 5.4.2.2.15 Budgets

The estimated budgets for the F-DPU considering the single box solution (e.g. two F-DPUs in one box) are shown below:

<table>
<thead>
<tr>
<th>Mass</th>
<th>&lt; 4.5 kg incl. margin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volume</td>
<td>270x270x110 mm</td>
</tr>
<tr>
<td>Power</td>
<td>2 x 10 W incl. losses in power converter</td>
</tr>
</tbody>
</table>

### 5.4.2.16 Technology Readiness Level

The current approach of the FEU considers relying on existing technologies and components. All required components already exist or will be available in near future in space-qualified (QML or similar) quality. In order to enable an early verification and validation of new interfaces (e.g. the FEE interface), the FEU development plan foresees in Phase A/B1 a prototype demonstrator. By following this approach, the proposed design can be validated very early and at minimum TRL5 will be achieved during Phase A/B1.
Assuming that the current design approach will be justified during Phase A/B1, the development of the FEU in Phase B2/C/D will be straightforward relying on existing technologies and components. Those technologies and components are already today at TRL8 or TRL9. Hence, a qualified FEU, representative for TRL8, will exist in Phase C without risk.

### 5.4.2.3 FGS ALGORITHMS

#### 5.4.2.3.1 Concept of data processing and algorithms

The attitude calculation of a telescope is based on the positions of stars on the CCD compared to the reference catalogue positions. Conventional star centroid algorithms using a single imagette achieve accuracies of about 1/10 of a pixel. Higher precisions can be obtained with information from accumulated measurements. In the case of PLATO a batch algorithm cannot be applied because attitude calculations are required for every time step (exposure). Furthermore jitter noise and differential aberration is expected which has to be modelled. Both can be done with a recursive filter structure. Therefore the proposed method is based on an extended Kalman filter (EKF) used for recursive nonlinear optimization.

Figure below shows an overview of the fine pointing algorithm providing attitude or error angle information for the AOCS. Every star centroid is estimated in a separate Kalman filter using a reduced star catalogue, camera model parameters and a motion model (attitude, angular rate) to predict the current position of the star on the CCD. This prediction is then updated with the actual measurement. All filtered star centroids are converted to observation vectors to calculate an optimal solution for the attitude of the fast telescope. With the last known orientation it is possible to update the angular rate. This is again done within a Kalman filter to reduce noise.

**FGS data processing overview**

- **Input**
  - CCD image
Initial Attitude, initial angular rate
Alignment to AOCS
Velocity vector for differential aberration
Reduced star catalogue
Precise camera model
- focal length
- principal point
- distortion parameters

Output (every 2.5 sec, minimum latency 100ms)
- Attitude quaternion $[q_0, q_1, q_2, q_3]$ incl. uncertainty
- Angular rate $[\omega]$
- Status (validity, time stamp, …)

5.4.2.3.2 Centroid calculation

A Kalman filter consists of a prediction step and a measurement update step. The prediction step is used to predict an a priori state $x$ from the a posteriori state $x^+$ and some state transition model $f$. It also calculates the a priori covariance $P^-$ with the a posteriori covariance and the gradient of the state transition model $F$. A model error $Q$ is also introduced. The a posteriori values are obtained from the precedent time step. For the first time step initialisation values can be incorporated.

$$x^- = f(x^+)$$
$$P^- = FP^+F^T + Q$$

The measurement step corrects the a priori state $x^-$ with new informations from the current measurement $z$ compared to the expected observation $h(x^-)$ from the a priori state. The Kalman gain $K$ is calculated to weight the information from the current measurements using $H$ the gradient of the observation equation and the measurement noise $R$.

$$x^+ = x^- + K(z - h(x^-))$$
$$K = P^-H^T(HP^-H^T + R)^{-1}$$
$$P^+ = (I - KH)P^-$$

For PLATO the prediction step is used to model the motion of a star centroid on the CCD plane due to some angular rate of the satellite. Starting with an initial rough orientation from AOCS an attitude ($q$) and an angular rate ($\omega$) is determined within calibration mode. The quaternion update assumes a constant or rather slow changing angular rate for the calculation of the attitude for the next time step.

$$q_k = \frac{1}{2}q_{k-1} \circ \bar{\omega} \quad \text{with} \quad \bar{\omega} = (0, \omega_x, \omega_y, \omega_z)^T$$

The selected star ($r$) is now rotated into the camera coordinate frame,

$$r' = q(k) \circ r \circ q(k)^*$$
and projected onto the CCD plane. A camera model with focal length $c_k$ and principal point $p_0$ is applied and corrected with a known distortion model ($\delta$).

$$x_0 = c_k \cdot \left( \frac{r'_x}{r'_z} + \delta_y \right) + p_{0x}$$

$$y_0 = c_k \cdot \left( \frac{r'_z}{r'_x} + \delta_y \right) + p_{0y}$$

This predicted centroid position is now filtered within the measurement update. It uses the following Gaussian PSF observations model to get the intensity distribution of the selected star window.

$$h = I_0 \sum_{i=1}^{m} \left[ \int \int dx \cdot e^{-\frac{(x-x_i)^2}{2\sigma_x^2}} \int dy \cdot e^{-\frac{(y-y_i)^2}{2\sigma_y^2}} + D \right]$$

with the centroid $(x_0, y_0)$, the intensity $I_0$ including the background $D$. For calculating the Kalman gain the Jacobian $H$ containing the gradients (partial derivatives) of all measurements $1...m$ is determined as follows.

$$H_m = \left( \frac{\partial h_m}{\partial x_0}, \frac{\partial h_m}{\partial y_0} \right)$$

By sub sampling (10x) the quaternion update the jitter noise is taken into account for the predicted intensity distribution as well as for the Jacobian.

### 5.4.2.3.3 Attitude Calculation

Using the camera model and the geometrical distortion model the filtered star centroids are transformed to vector observations $r'$ in the camera frame. With the corresponding reference vectors $r$ from a star catalogue the following optimization problem arises.

$$L(A) \equiv \frac{1}{2} \sum_i a_i \left[ r'_i - Ar_i \right]^2 \quad (i = 1,...,n)$$

Where $A$ is a orthogonal matrix (attitude matrix, direction-cosine matrix) and $a_i$ denoting non negative weights. This optimization problem is often refereed to as Wahba’s problem. It can be solved using Davenports q-Methode, which parameterizes the direction-cosine matrix by a unit quaternion.

$$A(q) = \left( q_i^2 - |q_i|^2 \right) I + 2q_i q_i^T - 2q_i [q_i, x]$$

The Problem is reduced it to an eigenvalue problem which can be solved very robustly. Another very efficient solution is implemented within the QUEST algorithm also solving for an optimal quaternion. See also RD4 for a more detailed discussion.

With two consecutive attitudes an angular rate is calculated, describing the movement of the camera frame. To increase the robustness against noise this calculation is also done within a Kalman filter.
5.4.2.3.4 AOCS algorithm performance simulation

To study the performance of the algorithm a simulation for a typical star field within 36.6 x 36.6 deg^2 has been performed. A start attitude was chosen and an overall angular rate of 1.5 arcsec/s applied to simulate jitter.

Several important cases have been simulated with special simulation software developed with as realistic as possible optical parameters. Simulation cases are:

Accuracy vs number of stars (with Gaussian PSF)

The goal is to find out how many stars are needed to achieve the required accuracy. Due to the limited data processing duty cycle or latency the number of stars should be low.

Accuracy vs PSF width (with Gaussian PSF)

The goal is to find out which PSF width (σ) is needed to achieve the required accuracy, or is σ=0.4 pixel (nominal optical image on CCD) sufficient.

Accuracy vs noise (with Gaussian PSF)

The goal is to find out which how robust is the algorithm against noise of CCD and electronics.

Robustness against geometrical distortion error (with Gaussian PSF)

The goal is to find out how robust is the algorithm against unknown geometrical optical distortion.

Accuracy with more realistic PSF generated by PLATOSIM (ZEMAX PSF)

The goal is to find out the accuracy of algorithm when using the for PLATO optics (first) representative PSF images.

The following inputs or parameters are used for simulation:

- TYCHO2 catalogue (2.5 million stars, m<12.5)
- Rectascension: 162°; Declination: 59°; Roll: 158.2°
- Angular rate: x: 1.125 arcsec/s; y: 0.65 arcsec/s; z: -0.75 arcsec/s
- CCD/Optics
  - Used mid array area: +/-9 deg (pixel 2255-6765 for each axis)
  - Principal point: centre CCD pixel {4510, 4510}
  - Focal length: tan(FOV/2)=0.34
  - Geometrical distortion: 1+0.05*r^2 (r normalized)
- The following noise terms were added (only for data not generated by PLATOSim).
  - Star intensity: ca. 10000DN for a star m = 4.8
  - Photon noise: 1DN (14bit) = 50 photons
5.4.2.3.5 Simulation example with PLATOSim imagettes

PLATOSim provides calibrated star PSF simulating the star PSF received by the onboard algorithms after transmissions by the telescope optics and integration by the CDD. These star imagettes are used as input of the processing algorithms for algorithm tuning and validation. Thus they are of interest in the validation of the FGS algorithm.

These imagettes will also be used for the DPS functional validation in order to demonstrate that after being processed by the DPS (EM and QM models), the science data in TM are the same as the data obtained during algorithm validation.

In order to use these imagettes for the FGS algorithm simulation, the jitter model should be updated to be representative of the SVM behaviour. The calibration model of the algorithm should also be updated to take into account the last updates of the camera design.

This work is ongoing. Once these updates performed, the PLATOSim imagettes will be used to validate the algorithm.

5.4.2.3.6 Summary of simulation results

A concept for a FGS pointing algorithm of the PLATO Fast-DPU is established. It shows that a recursive filter structure is necessary to fulfil the high accuracy requirements. The proposed algorithm is therefore based on Kalman filtering which allows for recursive state estimation of stochastically processes.

Changing attitude caused by an angular rate (Jitter noise and/or differential aberration) are identified to be a major source of error. A constant angular rate model is therefore introduced including a model error. This also allows slow changes of the angular rate. This model error will finally determine the accuracy of the algorithm. It is not limited by photon noise or read out noise.

As the algorithm is dependent on an accurate camera model including focal length, principal point and geometrical distortion, systematic errors in the model parameters will cause a decreased accuracy.

To verify the implemented algorithm a simulation was set up. A summary of the results are show in the table below.

<table>
<thead>
<tr>
<th>#</th>
<th>Simulation case</th>
<th>Accuracy result over 2.5sec</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Accuracy vs number of stars (with Gaussian PSF)</td>
<td>7 stars std = (0.015, 0.022, 0.087) arcsec/2.5sec</td>
<td>OK (7 stars)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>30 stars std = (0.019, 0.025, 0.049) arcsec</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Accuracy vs PSF width (with Gaussian PSF)</td>
<td>7 stars, $\sigma = 0.7$</td>
<td>OK (Defocusing needed $\sigma &gt; 0.7$)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>std = (0.015, 0.022, 0.087) arcsec/2.5sec</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>7 stars, $\sigma = 0.4$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>std = (0.056, 0.074, 0.492) arcsec/2.5sec</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Accuracy vs noise (with Gaussian PSF)</td>
<td>7 stars, $\sigma = 0.7$, noise = 2 DN</td>
<td>OK (robust against noise)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>std = (0.026, 0.046, 0.120) arcsec/2.5sec</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>7 stars, $\sigma = 0.7$, noise = 25 DN</td>
<td></td>
</tr>
</tbody>
</table>
Using Gaussian PSF shaped stars (case 1, 2, 3) it is shown that the algorithm fulfils the requirements of 0.032 arcsec/√Hz, which is 0.02 arcsec within 2.5 s (1/750 pixel).

A minimum of 7 stars (magnitude 4.88-5.33) within the inner CCD area (±9 deg) with a PSF width of 0.7 pixel is required. Increasing the number of stars will mainly have an influence on the roll angle accuracy (case 1). This could also be achieved using some stars from the outer area of the CCD.

The simulation shows (case 2) a significant drop in pointing data accuracy for a smaller PSF width. A defocusing of the Fast Telescopes is therefore recommended.

It is shown that the accuracy reached with the ZEMAX PSF (case 5) is slightly decreased but still close to the requirement as achieved with the Gaussian PSF simulation.

The needed processing power can be considered as not significant (or low) related to the available processing power with the planned F-DPU hardware design.

### 5.4.2.4 SOFTWARE ARCHITECTURE

The FEU software is divided into two parts. The Primary Boot Software (PBS, located in PROM) performs the Safe mode after power-on with the main goal to start the Application Software. The Application Software (APS, located in EEPROM) performs the Operational Modes after secondary boot from the Safe mode. The APS provides all the scientific functions of the F-DPU.

The PBS shall perform the following general tasks:

- Hardware initialization after power-on or reset
- On-Board time synchronization and TM time stamping
- Upload of the Application Software (APS) in EEPROM or RAM
- Start of the Application Software from EEPROM or RAM
- Maintaining and providing of EEPROM configuration information
- Maintaining of EEPROM APS boot segment information
- Memory management (up-/download) to EEPROM and RAM
- Providing of default housekeeping

From interface point of view the PBS has to handle the interface to the ICU. The PBS shall be realized as threaded application with a simple cooperative scheduler.

The APS shall perform the following general tasks:
- Check and execution of received telecommands
- Handling of instrument operational modes
- Receive data via RMAP from the Fast FEE
- AOCS data processing and interface handling (FGS algorithms)
- Science data Processing
- Instrument status monitoring, health check and event handling
- Send HK and science data as telemetry

From interface point of view the APS has to handle the ICU interface and the AOCS Interface. The data transfer from F-FFE to the F-DPU will be done by hardware. The APS shall be realized as an application running with the RTOS RTEMS.

Safety
For safety reasons the PBS which performs the Safe mode is a separate application stored in a rad-hard PROM.

A watchdog function will be implemented in order to re-start the F-DPU on-board software in case of malfunction due to damaging of the running application caused by single event upsets (SEU) in the ICU memory.

The APS is stored in an EEPROM device together with checksums for each segment. Before starting of APS the checksums will be re-calculated to make sure that the APS is correct.

Reliability
For realibility reasons a static memory table will be used (no dynamic memory allocation). As real time kernel of the APS a commercial proved stable RTOS will be used.

Maintainability
For maintainability reasons it is possible to upload a APS executable via command interface. The F-DPU on-board software is able to store and maintain up to three APS versions in order to have the possibility to go back to the farmer version for verification purposes. Additionally the parameters are separated
from the software code, to be maintained in EEPROM in a separate memory area also by uploading via commands (or TCs) from the ICU.

5.4.3 ICU

This section gives an overview of the ICU design.

5.4.3.1 REQUIREMENTS

Both ICUs (Main & Redundant) are gathered in a single box and work in cold redundancy. At a given instant, just one of the ICUs is active. In order to improve redundancy the 2 ICU chains (M+R) are implemented in the same box with the capability to cross-strap the main and redundant modules, owing to the use of a motherboard.

5.4.3.1.1 Common requirements

Each ICU shall implement the following common functions (non-exhaustive list):

- Handle the communication with spacecraft.
- Receive and process telecommands: the received commands will be validated prior to their execution.
- Format and transmit cyclic and sporadic HK telemetry packets (HKTM).
- Format and transmit the scientific payload telemetry packets (PLTM).
- Manage the SpaceWire network: the ICU is a remote network manager (router configuration, router monitoring, router status reporting...).
- Receive the onboard time (Central Time Reference) from the S/C, handle the time stamping of the data transmitted in HKTM and forward the CTR to the DPU.
- Receive a SpaceWire time code from the S/C and forward it to the DPU.
- Produce state and diagnosis information (cyclic status, progress event).
- Schedule the DPU tasks (by the way of commands sent to the DPU).
- Manage the data flow (especially in configuration mode).
- Manage the mode transitions.

- Manage the Software parameters.

- Manage the maintenance of the ICU software.

- Manage the maintenance of the N-DPU software.

- Manage the Star Catalogue.

- Compress the data using a lossless compression algorithm. A compression factor of at least 2 is required.

- Acquire and transmit to the S/C its own voltage and current consumptions.

5.4.3.1.2 Observation mode requirements

Every 2.5 sec., the active ICU processes the data (flux, centroids and imagettes) sent by the F-DPUs. The imagettes are compressed before being transmitted to the SVM. The flux and the centroids are stacked: N measurements are stacked for each F-DPU.

Every 25 sec., the active ICU processes the data (flux, centroids and imagettes) sent by the N-DPUs. The imagettes are compressed before being transmitted to the SVM. An outlier detection is performed on the flux and on the centroids by comparing the data corresponding to the same star as sent from N cameras (N=8 or N=16 or N=24 or N=32). The selection criterion is based on the computation of the median of the N measurements and on the variance computed at the 25-sec. cycle. The selected measurements are stacked.

Every 50 sec., the active ICU performs a detection of the outliers on the flux and on the centroids of the F-DPUs (criterion based on the computation of the median of the N stacked measurements and on the variance computed at the previous 50-sec. cycle). The mean and the variance of the k (k<=N) valid flux and centroids are computed. The computed data are bufferised waiting for compression and transmission to the SVM.

Every 50 sec., the active ICU also processes the stacked data corresponding to the N-DPU samples which are sent in TM at the cadence of 50 sec. The mean of the k (k <= M) valid stacked measurements (flux and centroids) are computed and bufferised waiting for compression and transmission to the SVM.
Every 600 sec., the active ICU processes the stacked data corresponding to the N-DPU samples which are sent in TM at the cadence of 600 sec. The mean and the variance of the \( k (k \leq L) \) valid stacked flux and centroids are computed and bufferised waiting for compression and transmission to the SVM.

For a more accurate description on memory budget and operations refer to Doc. Ref.: PLATO-INAF-ICU-RP-003 “ICU Memory Budget”.

5.4.3.1.3 Configuration mode requirements

In the configuration mode, the main functions of ICU are:

- Send the star catalogue and other configuration parameters to the DPUs.

- Cross check between data from telescopes of the same LoS (verify the consistency of the list and positions of all the stars).

- Compress full-frame images sent by the DPUs.

- Packetisation and transfer to SVM of all the data sent by DPU which allow to valid on-ground operations: "Far field" full images, list of background window positions and background intensities, coefficients associated with the background model, list and raw positions of candidate stars, list and accurate positions of reference stars, PSF parameters for all reference stars, distortion matrix, positions of all the targets, masks and window positions of all targets.

- No long-term storage of data (just temporary bufferisation).

5.4.3.2 DESIGN

This section reports on HW design of ICU and discuss on-data volumes and TM budgets.

5.4.3.2.1 Data volume and TM budget

The PLATO payload includes 32 normal cameras and 2 fast cameras, each equipped with 4 (4510 x 4510 pixels) CCDs. The expected data volume (adding 40% contingency) is roughly 212 Gb/day (imagettes, photometric data, centroid data, raw images, etc). Presently, the available TM rate is 106 Gb/day; so, ICU shall compress data by a factor of 2 at least.
ICU shall manage an input average data-rate from N-DPU and F-DPU of about 12 Mbps (16 x 735 kbps from the N-DPUs + 2 x 57 kbps from the F-DPUs) and an average output data-rate to the SVM of about 1.5 Mbps. These average data-rates can be easily managed by the standard SpW link, running up to 100 Mbps.

5.4.3.2.2 In-flight SW maintenance

As baseline ICU shall be in charge of the in-flight maintenance of the N-DPU application software (scientific SW) and its own SW. The N-DPU and ICU application software shall be reconfigurable during the flight, with the following possibilities:

- the software would be patched (partial SW modification);
- a new version of the application software would be uploaded on-board, entirely replacing the previous installed version;
- several versions of the application software could be stored on-board (the choice of the version shall be done by means of a dedicated TC).

The ICU and N-DPU application software shall be stored in a NOR FLASH EEPROM (Electrically-Erasable Programmable Read-Only Memory). The N-DPU boot protocol shall be based upon the RMAP protocol: no more PROM (and EEPROM) is needed at the DPU level (full hardware boot).

5.4.3.2.3 Analogue housekeeping acquisition and monitoring

ICU is responsible for acquiring its own voltage and current consumption and it shall also collect and transmit the HK data from the other subsystems.

The MEU-PSU subsystems are responsible for acquiring the voltage and current consumption of their own MEU (voltage and current consumption of each N-DPU board and of the router units). These HK data shall be collected by ICU through the SpW network.

Each fast or normal DPU shall receive the CCD and camera analog HKs (temperatures and voltages) from FEE. These analog HKs shall be transmitted to ICU through the SpW network.

The Fast DPUs, the 4 AEUs and the single F-AEU are responsible for acquiring their own voltage and current consumption. These HKs shall be sent to ICU through the SpW network.
5.4.3.2.4 HW architecture

The present ICU electronics architecture, proposed for the Definition Phase study, is an update of the design produced during the previous Assessment Phase and it includes some improvements concerning HW resources optimization. In order to manage the required SpW links, improve the SpW network reliability and the overall ICU cross-strapping capabilities we used three SpW routers in the so-called MEM&IO board, as input from 12 DPS links (4 MEU + 2 F-DPU + 4 AEU + 2 F-AEU SpW links) and as output to SVM (TM links) and a router in the Processor Unit as showed in the next figure.

Thanks to this new configuration the overall ICU (M+R) can benefit from a fully cross-strapped architecture, so any electronic configuration is available in case of failure of one or more subsystems.

Every subsystem function hosts at least a Control and Configuration FPGA interfacing one or more SpW Routers in order to manage communications and perform primary tasks, like writing and reading SDRAM memory modules by means of their own parallel ports and FIFO interfaces, as well described in the following sections.

The main tasks performed by the ICU SpW network are:

- to access ICU internal Memory Unit by means of the WR and RD Memory controller FPGAs and their parallel ports;
- to connect the Processing Unit 1 to the others Units;
- to connect the Processing Unit 2 (located in the redundant ICU) to the main network;
- to connect together the main and the redundant SpW multiplexing Units.

Two (M+R) independent SpW interfaces connect each ICU Processor board to the S/C OBC for TC reception and two (M+R) independent SpW interfaces connect each ICU MEM&IO board to the S/C Mass Memory for TM. Another SpW interface is provided for EGSE purposes. No SpW links between the ICU Processor Unit and the ICU-PSU have been included in the ICU design. They will be connected thanks to discrete line and/or serial interfaces.
ICU overall architecture block diagram (Main and Redundant).
5.4.3.2.5 Mechanical design and budgets

As baseline the ICU Unit (M+R) is composed by 3 nominal + 3 redundant daughter-board modules perpendicularly plugged onto a mother-board that lays on the unit bottom (2 Power Supply modules, 2 Processor modules, 2 MEM&IO modules).

The motherboard is fixed by screws to the unit bottom plate.

Each daughter-board is an extended double Eurocard module (233 mm x 200 mm) having motherboard connectors on one of the 233 mm side and with the external I/O connectors on the opposite side (TBC).

The daughter-boards are stiffened by a mechanical frame on which the external I/O connectors are fixed and screwed to the unit upper panels. The lateral sides of the modules support card-lock retainers that are used to fix the boards to the unit lateral panels.

All panels are made of aluminium alloy AL 7075 T7351 surface treated in ALODINE 1200 according to MIL-C-5541 CL. 3 and then externally painted in black CHEMGLAZE Z306 (except Bottom panel) to improve radiating exchange with the environment.

The thickness of the panels (1.5 mm reducible to 1 mm, after a realistic radiation environmental analysis related to L2) is designed to cope with the heat dissipation needs; in particular the thickness of the lateral panels increases from top to bottom to facilitate the heat sink.
5.4.3.2.5.1 Budgets

5.4.3.2.5.1.1 ICU composition

The proposed ICU is composed by the following boards:

<table>
<thead>
<tr>
<th>Board</th>
<th>Description</th>
<th>Qty</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Module</td>
<td>Hosting</td>
<td>1+1</td>
</tr>
<tr>
<td></td>
<td>SPV &amp; TC/TM DC/DC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>MEM&amp;IO DC/DC</td>
<td></td>
</tr>
<tr>
<td>Processor Module</td>
<td>Based on LEON2 Processor.</td>
<td>1+1</td>
</tr>
<tr>
<td></td>
<td>- 64MByte NOR FLASH EEPROM</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- 8MByte SRAM</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hosting TM acquisition</td>
<td></td>
</tr>
<tr>
<td>I/O &amp; Memory Module</td>
<td>- 2 Input SpW Router (12 users)</td>
<td>1+1</td>
</tr>
<tr>
<td></td>
<td>- 1 WR_Ctrl FPGA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- 1 MEM_Ctrl FPGA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- 1 RD_Ctrl FPGA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- 1 Output SpW Router</td>
<td></td>
</tr>
<tr>
<td></td>
<td>- 8 Gbit net usable memory array based on</td>
<td></td>
</tr>
<tr>
<td></td>
<td>256Mbit SDRAM TSOP assembled in cubes organized in</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(4+2) columns (Data+RS)</td>
<td></td>
</tr>
<tr>
<td>Motherboard</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

5.4.3.2.5.1.2 ICU power consumption

The ICU power consumption strongly depends on the overall maximum I/O throughput it has to sustain as well as on the used memory. A detailed estimation of maximum power consumption will be computed during the EBBs/EMs development once the above parameters will be definitely fixed (CPU clock rate, effective memory use, I/O throughput, etc).
At present the ICU overall power budget is as follows:

<table>
<thead>
<tr>
<th>Module</th>
<th>Power consumption [W]</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Module</td>
<td>2.9</td>
<td>85% min efficiency</td>
</tr>
<tr>
<td>Processor Module</td>
<td>6.1</td>
<td></td>
</tr>
<tr>
<td>I/O &amp; Memory Module</td>
<td>10.8</td>
<td>8Gbit</td>
</tr>
<tr>
<td>Motherboard</td>
<td>---</td>
<td></td>
</tr>
<tr>
<td><strong>Total Primary Power consumption</strong></td>
<td><strong>19.8</strong></td>
<td></td>
</tr>
</tbody>
</table>

### 5.4.3.2.5.1.3 ICU Mass Budget

The following table provides the Module Mass breakdown:

<table>
<thead>
<tr>
<th>Module</th>
<th>Unit Mass [g]</th>
<th>Qty</th>
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### 5.4.3.2.5.1.4 ICU Dimensions

The dimension of a Unit composed by:

- 2 Power Supply modules (1N+1R)
- 2 Processor modules (1N+1R)
- 2 MEM&IO modules (1N+1R)
- 1 Motherboard
are:

- 260 x 253 x 251 mm [L x W x H] not considering the mounting feet
- 260 x 278 x 251 mm [L x W x H] including the mounting feet

This dimensions are slightly larger than the requirements reported in the EID-B document (220 mm x 250 mm x 240 mm).

5.5 5.4.3.2.6 PROCESSOR MODULE

The Processor Module shall implement an AT697F (LEON2) SPARC V8 micro-processor with RTEMS OS (as baseline).

This Module is housed onto an extended double Eurocard PCB (200 mm x 233 mm) that is equipped with suitable connectors for internal connection to the Motherboard Unit and for I/O.

The ON/OFF switching of the Processor Module is achieved by switching on/off the associated DC/DC converter of the Power Supply module. The Processor Module with its own Monitoring Section and TM/TC capabilities perform the so-called Supervisor Function.

The processor includes on chip an Integer Unit (IU), a Floating Point Unit (FPU), a Memory Controller and a DMA Arbiter. Fault tolerance is supported using parity on internal/external buses and EDAC on the external data bus. Moreover the CPU itself provides:

- two 8-bits UART interfaces that can be used either for on-ground SW loading or for Debug with the SW Development & Maintenance facility;
- a Debug Support Unit;
- a J-TAG I/F, to interface the FPGA and the CPU.

The Processor Module hosts the following main functions.

5.4.3.2.6.1 Base Memory properties

128 KByte Boot Prom is provided for the bootstrap & initialisation SW.

64 MByte NOR FLASH EEPROM (2 x 16Mbit x 16 cubes with EDAC) is provided to store on board the ICU Application SW, the N-DPU ASW, the Star Catalogue and some configuration parameters. The
NOR FLASH memory is randomly addressed and can be fully patched and dumped during flight by means of telecommands. As baseline we assume that 64MB are sufficient to store 2 version of ICU Application SW and at least 4 version of N-DPUs Application SW, with the Star Catalogue (occupation less than 32MB).

8 MByte SRAM (2Mbit x 32 with EDAC) is provided for ICU Application SW execution.

Both FLASH EEPROM and SRAM are protected by the processor EDAC which corrects any single bit error and alert on any double bit error detected.

FLASH EEPROMs can be switched off when not accessed for long time in order to improve their data retention performance. The EEPROM On/Off switch is commanded through a GPIO line of the Processor.

5.4.3.2.6.2 SpaceWire I/F

The Processor Module host a 10X SpaceWire Router ASIC (ATMEL AT7910E) providing 8 SpW links and 2 parallel IFs.

3 SpW links are accessible from outside (2 used for TC purposes by SVM and 1 for EGSE) whilst the remaining SpW links are used for connection and cross strapping with other modules internal to the unit (Main and Redundant). 2 SpW links, used for TM, are provided by the MEM&IO board. The Processor Board SpW Router ASIC acts also as a network terminal node thanks to the two 8 bit wide parallel ports it provides.

The SpW links operate at 10Mbps in both directions (programmable rate; default at start up is 10Mbps).

5.4.3.2.6.3 Control & Communication FPGA

The Processor Module hosts a Control & Communication RTAX2000S FPGA gathering:

- clock division and distribution;

- OBT pre-settable binary counter;

- serial I/F controller;

- interrupt controller to expand interrupt capability;
- expansion logic providing General Purpose Output lines and Input lines;

- ADC IF to secondary voltages Monitoring logic.

5.4.3.2.6.4 Monitoring Function

The Processor Module also hosts a Monitoring Function subsystem interfacing the C&C FPGA to monitor the secondary voltages and currents as outputs from the Power Supply Module.

5.6 5.4.3.2.7 MEMORY AND IO MODULE

The MEM&IO Module is arranged on an extended double Eurocard PCB (220 mm x 233 mm). It is based on SDRAM memories that are assembled in 3D cubes.

The MEM&IO Module shall host (4+2) x 2Gbit Memory Cubes providing a usable memory capacity of 8Gbit. The I/F of such a Module are fully protected against failure propagation.

From the functional point of view the memory area is partitioned in sectors, being the sector the minimum area which can be allocated by the File Manager SW to a file/packet store. As baseline we consider a sector size of 1Mbyte.

The ICU proposed for PLATO hosts 2 fully independent MEM&IO Modules (1 operating and 1 cold back-up) each providing a net usable memory capacity up to 8Gbit.

5.4.3.2.7.1 Functions

The MEM&IO module can be powered on/off and controlled by the Processor module (either the nominal or the redundant one). This Module is composed by five main blocks:

- the Input Section with two SpW Routers (ATMEL AT7910E) and the WR_Ctrl FPGA;
- the Power Distribution and On/Off circuitry;
- the Memory Controller FPGA;
- the SDRAM Memory Array;
- the Output Section, composed by the RD_Ctrl FPGA with 1 SpW Router (ATMEL AT7910E).

The SDRAM Memory Array is split into (4+2) memory columns each composed by:
- 1 Latching Current Limiter;

- 16 Memory Cubes;

- the Buffer & Transceiver circuitry.

The Processor Module handles all the digital I/Fs of the MEM&IO and all the operations on the memory array: initialisation, writing, reading, refresh, scrubbing and the local redundancy management.

The memory operations are driven by the Supervisor Function in operational mode through the internal serial I/F. This allows command/reply transactions to perform remote read/write operations on the internal registers of the Memory controller FPGA but also on the whole SDRAM array.

The Memory Controller FPGA provides a dedicated controller of the serial I/F able to receive/process any command message and generate the corresponding reply message. Then, the serial I/F controller requests to the memory controller to perform physical access to the memory array.

5.4.3.2.7.2 Performances

As reported in the PLATO ICU Reference Documentation, strict constraints for the ICU HW design are: buffering large amount of data in order to achieve a stabilized compression factor of at least 2, handling a large number of SpW links from DPS (12) and implementing the on-board data compression algorithm in ICU.

So, to address these requirements, the total amount of SDRAM memory shall be at least 8 Gb as imposed by the size of the compression buffers, which dominates the budget. If this data is confirmed by the actual running simulations, the ICU MEM&IO Module consumption will be less than 11W.

The I/O Section of the MEM&IO Module host 3 SpW Routers and houses one Input Section and one Output Section.

The Input Section is the H/W support for all the storage operations during recording sessions; it consists of 3 main components: 1 Write Controller (WRCtl) FPGA and 2 SpW routers sending/receiving data to/from 12 SpW links of the DPS.
The Output module is the H/W support for all the retrieval operations during playback sessions; it consists of a Read Controller (RDCtrl) FPGA and 1 SpW router used as Downlink TM Channel to the SVM (2 TM links, M+R).

Each block can be independently switched on/off and has its own status line and interrupt line.

The **Input Section** consists of 4 main blocks:

- the WRCtrl FPGA (based on ACTEL RTAX2000) in charge of packets recording;
- two SpW routers (based on AT7910E ATMEL ASIC) in charge of the SpW I/F with the MEUs/AEUs, Nom/Red Supervisor module and with the two SpW routers of the redundant Input module;
- power Distribution and On/Off circuitry for the WRCtrl FPGA;
- two Power Distribution and On/Off circuitry for the two SpW Routers;

Each SpW router ASIC receives SpW packets from the external links towards DPS and routes them via its two parallel output ports to the WRCtrl FPGA, which stores them, on segment basis, into the addressed Packet Stores allocated inside the Memory Array.

The Input Section SpW routers (M+R) implement the symmetrical cross-strapping between each nom/red DPS I/F and the nom/red WRtrlC FPGA on the unit.

Failure propagation is prevented on any internal I/F, cross-strapping I/F and instrument I/F, no matter the on/off status of each block.

The Input Module Section automatically:

- route to the output parallel ports (towards the WRCtrl FPGA) all the SpW (TM) packets they have received from the DPS and Processor Module;
- route on their SpW ports all the SpW (TC) packets generated by the OBC for the cameras chain and ancillary electronics;
- propagate towards DPS, via SpW link, the time-codes generated by the OBC to synchronize their OBT with that of the OBC.
The **Output Section** consists of 4 main blocks:

- ✓ the RDCtrl FPGA (based on ACTEL RTAX2000) in charge of packets retrieval;
- ✓ 1 SpW router (based on AT7910E ATMEL ASIC) in charge of the SpW I/F with the 2 TM downlink channels and with the SpW router of the redundant Output Section;
- ✓ power Distribution and On/Off circuitry for the RDCtrl FPGA;
- ✓ power Distribution and On/Off circuitry for the SpW Router.

The RDCtrl FPGA retrieves TM packets allocated inside the Memory Array via parallel output ports, formats them into SpW packets and forwards them to SVM. The Output Routers (M+R) implement the symmetrical cross-strapping between each nom/red MEM&IO Module.

The tasks performed by the SpW Router on the host RDCtrl FPGA can be configured/controlled/monitored by the active Processor Module.

The WRCtrl and RDCtrl FPGA operations can be configured/controlled/monitored by the operational supervisor function of the unit, via the associated serial I/Fs. Nom. and red. I/Fs are OR-ed inside the input sections. All the I/Fs are protected against failure propagation.

### 5.7 5.4.3.2.8 POWER SUPPLY MODULE

The Power Supply module, which is implemented on an extended double Eurocard PCB (200 mm x 233 mm), provides independent power supply to the two main functional blocks composing the unit:

- ✓ the Processor Module performing the Supervisor Function;
- ✓ the MEM&IO Module.

Therefore this module hosts two independent DC/DC Converters named SPV_DC/DC and MEM&IO_DC/DC.

Redundancy is achieved by using two of these Power Supply modules. Each DC/DC converters can operate with a primary power bus in the range 23 ÷ 38V.

Each DC/DC Converter can be individually switched ON/OFF: the SPV_DC/DC by means of external (from SVM) redundant Standard High Power ON/OFF commands while the MEM&IO_DC/DC by means of internal redundant low level commands generated by the Processor Modules.
Monitoring signals (that are secondary voltages, currents and temperatures) are provided to the Processor Module to be acquired (i.e conditioned and A/D converted) by a Monitoring Section and C&C FPGA on the CPU board.

Both SPV_DC/DC and MEM&IO_DC/DC provide the following features:

- Electrical isolation between primary input and secondary output voltages
- EMI filtering (common and differential mode)
- Inrush current limiting
- Latching overcurrent protection (Overload)
- Input voltage polarity inversion protection
- Input undervoltage protection
- Output overvoltage protection
- ON/OFF capability via either external HPC or internal commands
- ON/OFF status monitoring
- Secondary output voltage monitoring
- Hot spot temperature monitoring

5.8 5.4.3.2.9 MOTHERBOARD

The Motherboard is the mean through which the Nominal and Redundant Daughter-boards are connected and exchange the power and signal lines each other. Owing to using a motherboard PCB, there are no wire connections inside the ICU Unit.

As a matter of fact all the I/O connectors are directly mounted on the relevant PCB modules.

The Motherboard is equipped with straight connectors and lies on the unit bottom panel while the Daughter-boards are inserted through the top of the unit and plug onto the Motherboard through right-angle connectors.
5.4.3.3 SW DESCRIPTION

5.4.3.3.1 SW general description

There are 4 kinds of SW available to the ICU: the Bootstrap SW (BSW), the operating system (OS), the drivers and the Application SW (ASW). The BSW and the drivers are provided by the ICU HW manufacturer; the OS depends on the adopted microprocessor but anyway will be a real-time OS commercially available, RTEMS as baseline. The drivers will be developed to be integrated in the OS. The ASW is under responsibility of IFSI-INAF. The ASW code shall be written in C; some module may be required to be written in Assembly.

The SW can also be seen as structured in layers; each layer offering services to the upward layer and exploits the services of the downward one; this add a “vertical” modularity to the SW approach which fosters portability and maintenance.

The SW is implemented following ECSS-E40 Part 1, as outlined in the Guide to applying the ESA software engineering standards to small software projects (BSSC(96)2, Issue 1. May 1996), ECSS-E-70-41A standards and PUS based applications.

![SW layer structure.](image)

5.4.3.3.2 SW Layer Description

The lowest level layer is the Board Support Package which maps the boards registers structure and supplies the routines needed to configure them. The HW Handlers layer holds the support code to perform basic operations on the HW, it also include the routines mapping the asynchronous interrupts generated by the modules.

RTEMS (Real-Time Executive for Multiprocessor Systems) is a real-time operating system designed for embedded systems. The directive execution times and other critical performance parameters such as
interrupt latency are comparable to those of commercial executives. RTEMS offers very low overhead with usable configurations well under 32K and is deterministic with guaranteed execution times for nearly every operation.

The Basic SW, though separated, can also be considered as a part of ASW because it includes the services needed to fulfil the mission requirements, like: File Allocation Table management, memory patch and dump, memory scrubbing, SpW link management and so on.

The Application SW is the uppermost layer which interfaces the OBC and the DPS or camera chains. It implements the functions described by the high level mission requirements with a modular architecture.

5.4.3.3.2.1 Bootstrap

The Start-up phase starts with the power-on of the unit and the CPU start to execute the code in the PROM including basic unit initialisations. The Bootstrap SW consists mainly of two components: ROM_Boot and RAM_Boot.

After switch-on the unit goes into POWER-ON mode: the ROM_Boot code is running to perform the basic tests and to copy RAM_Boot application from PROM to RAM. The tests performed at the ROM_Boot phase are:

- initialise test Boot Results Area;
- RAM Boot Area test;
- Processor Board test: checks as much as possible of the HW (interrupt lines, EDAC, failure detection capabilities).

Then the execution continues in RAM. The RAM_Boot completes the tests then load the SecurePD application from PROM to RAM. The tests performed at the RAM_Boot phase are:

- RAM addressing and pattern retention test: checks that all writes to RAM cells fits in the correct place with the right value, leaves the memory blanked;
- PROM CRC check: computes the CRC value of the PROM area and compares it with the value stored in the PROM itself;
- ASW images in FLASH EEPROM CRC check: computes the CRC value of both ASW images stored in EEPROM and compares the results with the values stored in the EEPROM itself.
A little area, at the end of RAM, stores both the information related to Bootstrap Built-in test (BIT) results and the transitions log between the Operating Modes. The execution of a test is conditioned by the successful result of the execution of the previous test; in other words, if a test fails, all the successive tests are skipped.

5.4.3.3.2 SecurePD SW

The SecurePD SW is a compact application (without OS presence), stored in PROM, which provides few basic functionalities to allow (re)load and dump of unit memory.

The SecurePD remain active until a telecommand commanding a Mode Transition function, is received, requesting to switch to IDLE mode: in this case SecurePD will load the first good ASW image from FLASH EEPROM to RAM and start the execution of it.

The SecurePD SW will be executed in following conditions:

- at unit switch-on, after Bootstrap phase (POWER-ON mode);
- each time that LEON2 Watchdog expires;
- on processor HW error;
- on Warm Reset (due to a recovery action or Reboot TC): in this case the tests doesn't erase the RAM and its content can be observed.

5.4.3.3.3 Application SW

From the point of view of the OS, the application SW can be seen as a set of procedures, or tasks, whose execution starts on the reception of a HW or SW interrupt. Hereafter we give a list of functional high level requirements upon which the SW will be developed: each requirement will be implemented with one or more routines that will be logically integrated in the different tasks.

The ICU shall:

- Handle the communication with the SVM;
- Handle the communication with the DPUs, nominal and fast;
- Receive and process the TCs sent from the SVM;
- By mean of commands sent to the DPUs, ensure an overall coordination of activities among the DPUs, e.g. selecting an operating mode common to all the subunits. This configuration shall be started by commands received from the SVM;
✓ Manage the data flow from/to DPUs and from/to SVM;
✓ Format and transmit to SVM the ICU and DPUs HKTM: SW status, DPUs HW status, command acknowledgments, memory dumps, event reports, failure reports, etc;
✓ Format and transmit to the SVM the scientific packets (PLTM). The scientific packets can contain light curves, centroid curves, imagettes or full frame images;
✓ Handle the absolute time-stamping of HKTM and PLTM on the basis of the time information received from the SVM; if required propagate the time info to the subunits;
✓ Produce state and diagnosis information; in case of out-of-limit conditions start pre-defined on board procedures to preserve the integrity of the instrument;
✓ Manage mode changes on the base of commands from the SVM;
✓ Manage the maintenance of the ICU application software (memory check / dump / upload);
✓ Support the maintenance of the N-DPUs application software.

Data compression is a fundamental task of the ASW: it will be developed by the University of Wien and will be integrated in the ICU SW. ASW validation will be done by IFSI-INAF.

6. PAYLOAD TECHNICAL BUDGETS AND CONCLUSION

The technical budgets of the payload, i.e. power budget, mass budget and telemetry budget are given in the Payload Performance Report [AD3].

The present design is fully compatible with the requirements of these budgets, with the required margins of 20%.

A compliance table with the scientific requirements is also given in the Payload Performance Report. It shows that the present design is compliant or partially compliant with all scientific requirements.
### DISTRIBUTION LIST

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<td>Fundación Galileo Galilei - INAF</td>
<td>Rambla José Ana Fernández Pérez, 7</td>
<td>38712 Breña Baja, TF - Spain</td>
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<tr>
<td>COSENTINO Rosario</td>
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<td>GALLE Stéphane</td>
<td><a href="mailto:stephane.gallet@lidax.com">stephane.gallet@lidax.com</a></td>
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### DIFFUSION MSSL

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<td><a href="mailto:prg@mssl.ucl.ac.uk">prg@mssl.ucl.ac.uk</a></td>
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<td>SMITH Alan</td>
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<td>WALTON David</td>
<td><a href="mailto:dmw@mssl.ucl.ac.uk">dmw@mssl.ucl.ac.uk</a></td>
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### DIFFUSION Università di PADOVA

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### DIFFUSION University of Lisbon

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